

Memories

MOS, TTL, ECL

Elcoma – Philips Electronic Components and Materials Division – embraces a world-wide group of companies operating under the following names:

IBRAPE



Miniwatt

Signetics

Mullard

VALVO

PHILIPS

Elcoma offers you a technological partnership in developing your systems to the full. A partnership to which we can bring

- world-wide production and marketing
- know-how
- systems approach
- continuity
- broad product line
- fundamental research
- leading technologies
- applications support
- quality

MEMORIES
MOS, TTL, ECL

	<i>page</i>
Selection guide	1
Functional index	3
Numerical index	5
MOS Memories	9
Introduction	11
Type designation	13
Rating systems	15
Handling MOS devices	16
CMOS RAM	17
CMOS EEPROM	111
Charge-Coupled Memory	121
TTL Memories	131
Introduction	133
Quality and Reliability	134
Selection Guide	140
PROM Cross Reference Guide	142
RAM Cross Reference Guide	144
Ordering Information	145
64-bit RAM	147
256-bit RAM	157
Byte-Organized RAM	175
PROM Programming Information	195
Low Complexity PROM	199
4K-bit PROM	225
8K-bit PROM	241
16K-bit PROM	271
32K-bit PROM	283
64K-bit PROM	291
ECL Memories	297
ECL RAM	299
Package information	323

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.

Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

- T1** **Tubes for r.f. heating**
- T2a** **Transmitting tubes for communications, glass types**
- T2b** **Transmitting tubes for communications, ceramic types**
- T3** **Klystrons**
- T4** **Magnetrons for microwave heating**
- T5** **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6** **Geiger-Müller tubes**
- T8** **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units
- T9** **Photo and electron multipliers**
- T10** **Plumbicon camera tubes and accessories**
- T11** **Microwave semiconductors and components**
- T12** **Vidicon and Newvicon camera tubes**
- T13** **Image intensifiers and infrared detectors**
- T15** **Dry reed switches**
- T16** **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

- S1 Diodes**
Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
- S2a Power diodes**
- S2b Thyristors and triacs**
- S3 Small-signal transistors**
- S4a Low-frequency power transistors and hybrid modules**
- S4b High-voltage and switching power transistors**
- S5 Field-effect transistors**
- S6 R.F. power transistors and modules**
- S7 Surface mounted semiconductors**
- S8a Light-emitting diodes**
- S8b Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components
- S9 Power MOS transistors**
- S10 Wideband transistors and wideband hybrid IC modules**
- S11 Microwave transistors**
- S12 Surface acoustic wave devices**
- S13 Semiconductor sensors**
- *S14 Liquid Crystal Displays**

*To be issued shortly.

INTEGRATED CIRCUITS (PURPLE SERIES)

The NEW SERIES of handbooks is now completed. With effect from the publication date of this handbook the "N" in the handbook code number will be deleted.

Handbooks to be replaced during 1986 are shown below.

The purple series of handbooks comprises:

IC01	Radio, audio and associated systems Bipolar, MOS	new issue 1986 IC01N 1985
IC02a/b	Video and associated systems Bipolar, MOS	new issue 1986 IC02Na/b 1985
IC03	Integrated circuits for telephony Bipolar, MOS	new issue 1986 IC03N 1985
IC04	HE4000B logic family CMOS	new issue 1986 IC4 1983
IC05N	HE4000B logic family – uncased ICs CMOS	published 1984
IC06N	High-speed CMOS; PC74HC/HCT/HCU Logic family	published 1986
IC08	ECL 10K and 100K logic families	New issue 1986 IC08N 1984
IC09N	TTL logic series	published 1986
IC10	Memories MOS, TTL, ECL	new issue 1986 IC7 1982
IC11N	Linear LSI	published 1985
Supplement to IC11N	Linear LSI	published 1986
IC12	I²C-bus compatible ICs	not yet issued
IC13	Semi-custom Programmable Logic Devices (PLD)	new issue 1986 IC13N 1985
IC14N	Microprocessors, microcontrollers and peripherals Bipolar, MOS	published 1985
IC15	FAST TTL logic series	new issue 1986 IC15N 1985
IC16	CMOS integrated circuits for clocks and watches	first issue 1986
IC17	Integrated Services Digital Networks (ISDN)	not yet issued
IC18	Microprocessors and peripherals	new issue 1986*

* The Microprocessors were included in handbook IC14N 1985, so IC18 will replace that part of IC14N.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

- C2** Television tuners, coaxial aerial input assemblies, surface acoustic wave filters
- C3** Loudspeakers
- C4** Ferroxcube potcores, square cores and cross cores
- C5** Ferroxcube for power, audio/video and accelerators
- C6** Synchronous motors and gearboxes
- C7** Variable capacitors
- C8** Variable mains transformers
- C9** Piezoelectric quartz devices
- C11** Varistors, thermistors and sensors
- C12** Potentiometers, encoders and switches
- C13** Fixed resistors
- C14** Electrolytic and solid capacitors
- C15** Ceramic capacitors
- C16** Permanent magnet materials
- C17** Stepping motors and associated electronics
- C18** Direct current motors
- C19** Piezoelectric ceramics
- C20** Wire-wound components for TVs and monitors
- C22** Film capacitors

SELECTION GUIDE

Functional index.....	3
Numerical index.....	5

FUNCTIONAL INDEX

type number	description	page
CMOS RAM		
PCD5101	256 x 4-bit static RAM	19
PCD5114	1024 x 4-bit static RAM	27
PCF8570	256 x 8-bit static RAM with I ² C bus interface	35
PCF8571	128 x 8-bit static RAM	47
PCF8583	256 x 8-bit static RAM	59
HEF4505B	64-bit, 1-bit per word R/W RAM	77
HEF4720B; V	256-bit, 1-bit per word RAM	85
SBB6116L-10	2048 x 8-bit static RAM; max. access time 100 ns	101
SBB6116L-12	2048 x 8-bit static RAM; max. access time 120 ns	101
CMOS EEPROM		
PCB8582	Static CMOS EEPROM (256 x 8)	113
Charge-Coupled Memory		
SAA9001	317K-bit CCD memory	123
64-bit TTL Bipolar RAM		
82S25	64-bit Bipolar RAM (16 x 4)	149
3101A	64-bit Bipolar RAM (16 x 4)	149
74F189	64-bit Bipolar RAM (16 x 4)	153
74S189	64-bit Bipolar RAM (16 x 4)	149
256-bit TTL Bipolar RAM		
82S16	256-bit Bipolar RAM (256 x 1)	159
82LS16	256-bit Bipolar RAM (256 x 1)	163
74S301	256-bit Bipolar RAM (256 x 1)	167
74LS301	256-bit Bipolar RAM (256 x 1)	171
Byte-Organized RAM		
82S09/82S09A	576-bit Bipolar RAM (64 x 9)	177
82S19	576-bit Bipolar RAM (64 x 9)	181
82S212/82S212A	2304-bit Bipolar RAM (256 x 9)	185
8X350	2048-bit Bipolar RAM (256 x 8)	189

FUNCTIONAL INDEX

type number	description	page
Low Complexity PROM		
82S23/82S123	256-bit Bipolar PROM (32 x 8)	201
82S23A/82S123A	256-bit Bipolar PROM (32 x 8)	204
82S126/82S129	1024-bit Bipolar PROM (256 x 4)	207
82S126A/82S129A	1024-bit Bipolar PROM (256 x 4)	210
82S130/82S131	2048-bit Bipolar PROM (512 x 4)	213
82S130A/82S131A	2048-bit Bipolar PROM (512 x 4)	216
82S135	2048-bit Bipolar PROM (256 x 8)	219
82LS135	2048-bit Bipolar PROM (256 x 8)	222
4K-bit TTL Bipolar PROM		
82S115	4096-bit Bipolar PROM (512 x 8)	227
82S137	4096-bit Bipolar PROM (1024 x 4)	231
82S137A/82S137B	4096-bit Bipolar PROM (1024 x 4)	234
82S147/82S147A	4096-bit Bipolar PROM (512 x 8)	237
8K-bit TTL Bipolar PROM		
82S181	8192-bit Bipolar PROM (1024 x 8)	243
82S181C	8192-bit Bipolar PROM (1024 x 8)	246
82LS181	8192-bit Bipolar PROM (1024 x 8)	249
82S183	8192-bit Bipolar PROM (1024 x 8)	252
82S185	8192-bit Bipolar PROM (2048 x 4)	256
82S185A/82S185B	8192-bit Bipolar PROM (2048 x 4)	259
82HS187/82HS187A	8192-bit Bipolar PROM (1024 x 8)	262
82HS189/82HS189A	8192-bit Bipolar PROM (1024 x 8)	266
16K-bit TTL Bipolar PROM		
82S191/82S191A	16,384-bit Bipolar PROM (2048 x 8)	273
82S191C	16,384-bit Bipolar PROM (2048 x 8)	276
82HS195/82HS195A/82HS195B	16,384-bit Bipolar PROM (4096 x 4)	279
32K-bit TTL Bipolar PROM		
82S321	32,768-bit Bipolar PROM (4096 x 8)	285
82HS321/82HS321A/82HS321B	32,768-bit Bipolar PROM (4096 x 8)	288
64K-bit TTL Bipolar PROM		
82HS641/82HS641A/82HS641B	65,536-bit Bipolar PROM (8192 x 8)	293
Bipolar ECL RAM		
10422B	256 x 4-bit RAM	301
10422C	256 x 4-bit RAM	304
10470A	4096 x 1-bit RAM	307
100422B	256 x 4-bit RAM	310
100422C	256 x 4-bit RAM	313
100470A	4096 x 1-bit RAM	316
100474A	1024 x 4-bit RAM	319

NUMERICAL INDEX

type number	description	page
HEF4505B	64-bit, 1-bit per word R/W RAM	77
HEF4720B; V	256-bit, 1-bit per word RAM	85
PCB8582	Static CMOS EEPROM (256 x 8)	113
PCD5101	256 x 4-bit static RAM	19
PCD5114	1024 x 4-bit static RAM	27
PCF8570	256 x 8-bit static RAM with I ² C bus interface	35
PCF8571	128 x 8-bit static RAM	47
PCF8583	256 x 8-bit static RAM	59
SAA9001	317K-bit CCD memory	123
SBB6116L-10	2048 x 8-bit static RAM; max. access time 100 ns	101
SBB6116L-12	2048 x 8-bit static RAM; max. access time 120 ns	101
8X350	2048-bit Bipolar RAM (256 x 8)	189
74F189	64-bit Bipolar RAM (16 x 4)	153
74LS301	256-bit Bipolar RAM (256 x 1)	171
74S189	64-bit Bipolar RAM (16 x 4)	149
74S301	256-bit Bipolar RAM (256 x 1)	167
82HS187/82HS187A	8192-bit Bipolar PROM (1024 x 8)	262
82HS189/82HS189A	8192-bit Bipolar PROM (1024 x 8)	266
82HS195/82HS195A/82HS195B	16,384-bit Bipolar PROM (4096 x 4)	279
82HS321/82HS321A/82HS321B	32,768-bit Bipolar PROM (4096 x 8)	288
82HS641/82HS641A/82HS641B	65,536-bit Bipolar PROM (8192 x 8)	293
82LS16	256-bit Bipolar RAM (256 x 1)	163
82LS135	2048-bit Bipolar PROM (256 x 8)	222
82LS181	8192-bit Bipolar PROM (1024 x 8)	249
82S09/82S09A	576-bit Bipolar RAM (64 x 9)	177
82S16	256-bit Bipolar RAM (256 x 1)	159
82S19	576-bit Bipolar RAM (64 x 9)	181
82S23/82S123	256-bit Bipolar PROM (32 x 8)	201
82S23A/82S123A	256-bit Bipolar PROM (32 x 8)	204
82S25	64-bit Bipolar RAM (16 x 4)	149
82S115	4096-bit Bipolar PROM (512 x 8)	227
82S126/82S129	1024-bit Bipolar PROM (256 x 4)	207
82S126A/82S129A	1024-bit Bipolar PROM (256 x 4)	210
82S130/82S131	2048-bit Bipolar PROM (512 x 4)	213
82S130A/82S131A	2048-bit Bipolar PROM (512 x 4)	216
82S135	2048-bit Bipolar PROM (256 x 8)	219
82S137	4096-bit Bipolar PROM (1024 x 4)	231
82S137A/82S137B	4096-bit Bipolar PROM (1024 x 4)	234
82S147/82S147A	4096-bit Bipolar PROM (512 x 8)	237
82S181	8192-bit Bipolar PROM (1024 x 8)	243

NUMERICAL INDEX

type number	description	page
82S181C	8192-bit Bipolar PROM (1024 x 8)	246
82S183	8192-bit Bipolar PROM (1024 x 8)	252
82S185	8192-bit Bipolar PROM (2048 x 4)	256
82S185A/82S185B	8192-bit Bipolar PROM (2048 x 4)	259
82S191/82S191A	16,384-bit Bipolar PROM (2048 x 8)	273
82S191C	16,384-bit Bipolar PROM (2048 x 8)	276
82S212/82S212A	2304-bit Bipolar RAM (256 x 9)	185
82S321	32,768-bit Bipolar PROM (4096 x 8)	285
3101A	64-bit Bipolar RAM (16 x 4)	149
10422B	256 x 4-bit RAM	301
10422C	256 x 4-bit RAM	304
10470A	4096 x 1-bit RAM	307
100422B	256 x 4-bit RAM	310
100422C	256 x 4-bit RAM	313
100470; A	4096 x 1-bit RAM	316
100474A	1024 x 4-bit RAM	319

MOS MEMORIES

Introduction 11
CMOS RAM 17
CMOS EEPROM111
Charge-Coupled Memory121

Introduction

Type designation	13
Rating systems	15
Handling MOS devices	16

PRO ELECTRON TYPE DESIGNATION CODE
FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic type number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER**1. DIGITAL FAMILY CIRCUITS**

The **FIRST TWO LETTERS** identify the **FAMILY** (see note 1).

2. SOLITARY CIRCUITS

The **FIRST LETTER** divides the solitary circuits into:

- S : Solitary digital circuits
- T : Analogue circuits
- U : Mixed analogue/digital circuits

The **SECOND LETTER** is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 3).

3. MICROPROCESSORS

The **FIRST TWO LETTERS** identify microprocessors and correlated circuits as follows:

- MA : { Microcomputer
- { Central processing unit
- MB : Slice processor (see note 2)
- MD : Correlated memories
- ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The **FIRST TWO LETTERS** identify the following:

- NH : Hybrid circuits
- NL : Logic circuits
- NM : Memories
- NS : Analogue signal processing, using switched capacitors
- NT : Analogue signal processing, using CTDs
- NX : Imaging devices
- NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.
3. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

TYPE DESIGNATION

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

- A : temperature range not specified
- B : 0 to + 70 °C
- C : -55 to + 125 °C
- D : -25 to + 70 °C
- E : -25 to + 85 °C
- F : -40 to + 85 °C
- G : -55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

- C : for cylindrical
- D : for ceramic DIL
- F : for flat pack
- L : for chip on tape
- P : for plastic DIL
- Q : for QIL
- T : for miniature plastic (mini-pack)
- U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

- C : Cylindrical
- D : Dual-in-line (DIL)
- E : Power DIL (with external heatsink)
- F : Flat (leads on 2 sides)
- G : Flat (leads on 4 sides)
- K : Diamond (TO-3 family)
- M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
- Q : Quadruple-in-line (QIL)
- R : Power QIL (with external heatsink)
- S : Single-in-line
- T : Triple-in-line
- W : Lead chip-carrier (LCC)
- X : Leadless chip-carrier (LLCC)
- Y : Pin grid array (PGA)

SECOND LETTER: Material

- C : Metal-ceramic
- G : Glass-ceramic (cerdip)
- M : Metal
- P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device.

An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

Characteristic

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating

A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

Rating system

The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.

Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

CMOS RAM

PCD5101	256 x 4-bit static RAM	19
PCD5114	1024 x 4-bit static RAM	27
PCF8570	256 x 8-bit static RAM	35
PCF8571	128 x 8-bit static RAM	47
PCF8583	256 x 8-bit static RAM	59
HEF4505B	64-bit, 1-bit per word R/W RAM.	77
HEF4720B; V	256-bit, 1-bit per word RAM.	85
SBB6116L-10; 12	2048 x 8-bit static RAM	101

256 × 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5101 is a very low-power 1024-bit static CMOS random access memory, organized as 256 words by 4 bits. It is suitable for low power and high speed applications where battery standby power is required to ensure non-volatility of data. All inputs and outputs are fully TTL compatible and pinning is compatible with 2101-type NMOS static RAMs and 5101-type CMOS static RAMs.

There are two chip enable inputs, $\overline{CE1}$ and $\overline{CE2}$, selection being made when $\overline{CE1}$ is LOW and $\overline{CE2}$ is HIGH. The memory has an output disable function, OD, which allows the inputs/outputs to be used separately, or to be tied together for use in common data I/O systems.

Features

- Operating supply voltage range
- Low data retention voltage
- Low power consumption in both operating and standby modes
- Access time 150 ns at $V_{DD} = 5\text{ V}$; 400 ns at $V_{DD} = 3\text{ V}$
- Three-state outputs
- All inputs and outputs directly TTL compatible
- Choice of two package types

2,5 to 5,5 V
min. 1 V

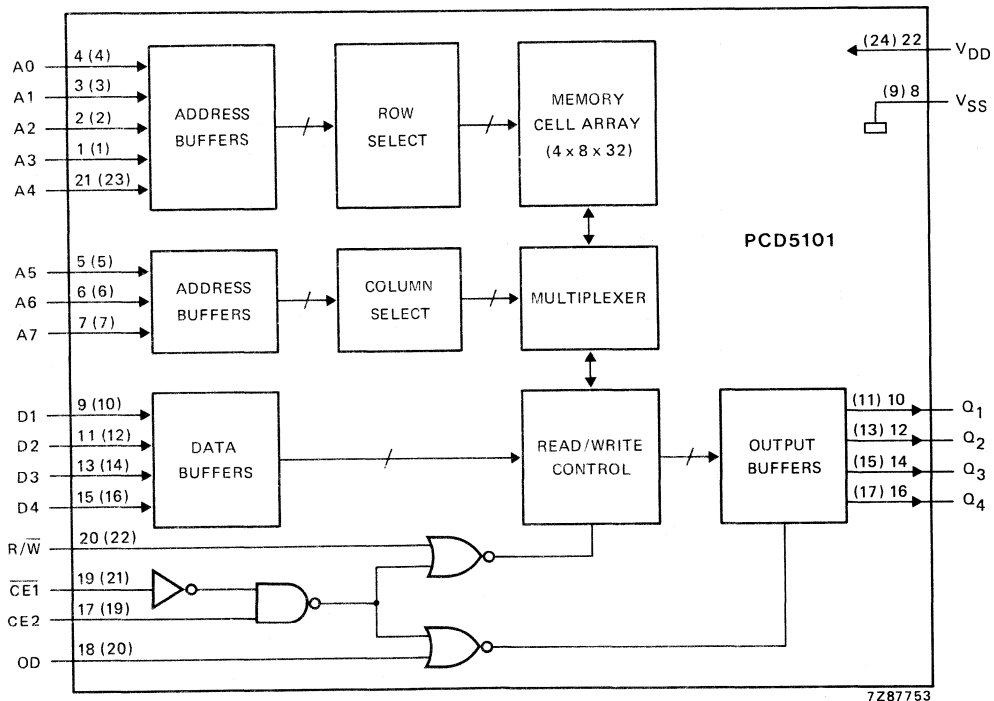


Fig. 1 Block diagram: pin numbers in parentheses are for PCD5101T; other pin numbers are applicable to PCD5101P.

PACKAGE OUTLINES

PCD5101P: 22-lead DIL; plastic (SOT-116).

PCD5101T: 24-lead mini-pack, plastic (SO-24; SOT-137A).

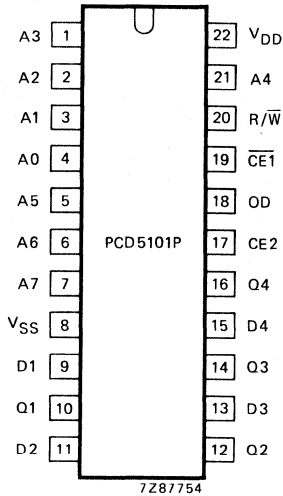


Fig. 2 Pinning diagram for PCD5101P.

PINNING

- D1 } data inputs
- D2 }
- D3 }
- D4 }
- A0 } address inputs
- A1 }
- A2 }
- A3 }
- A4 }
- A5 }
- A6 }
- A7 }
- R/ \bar{W} read/write input
- $\overline{CE1}$ } chip enable inputs
- CE2 }
- OD output disable
- Q1 } data outputs
- Q2 }
- Q3 }
- Q4 }
- V_{DD} positive supply
- V_{SS} negative supply
- n.c. not connected

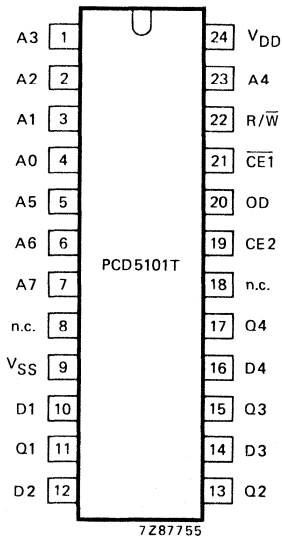


Fig. 3 Pinning diagram for PCD5101T.

OPERATING MODES

Table 1 Mode selection

$\overline{CE1}$	CE2	R/ \overline{W}	OD	mode of operation	output state
H	X	X	X	standby	high impedance
X	L	X	X	standby	high impedance
L	H	L	H	write	high impedance
L	H	L	L	write	equal to input data
L	H	H	L	read	data valid
L	H	H	H	read	high impedance

Separate input/output: write cycle OD = X; read cycle OD = L.

Common input/output: write cycle OD = H; read cycle OD = L.

H = HIGH voltage level

L = LOW voltage level

X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	-0,3 to 8,0 V
Input voltage range (any pin)	V_I	$V_{SS} - 0,3$ to $V_{DD} + 0,3$ V
Operating temperature range	T_{amb}	-25 to +70 °C
Storage temperature range	T_{stg}	-55 to +125 °C

D.C. CHARACTERISTICS ($V_{DD} = 5\text{ V}$) $V_{DD} = 5 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to }+70\text{ }^{\circ}\text{C}$

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5,0	5,5	V
Operating supply current at $V_I = V_{DD}$ or V_{SS} ; $f = 1\text{ MHz}$; outputs open	I_{DD}	—	10	17	mA
at $V_I = 0,8$ or $2,0\text{ V}$; $f = 1\text{ MHz}$; outputs open	I_{DD}	—	10	17	mA
at $V_I = 0,8$ or $2,0\text{ V}$; $f = 5\text{ MHz}$; outputs open	I_{DD}	—	12	20	mA
Standby supply current at $CE2 = V_{SS}$	I_{SB}	—	0,02	5,0	μA
Input leakage current at $V_I = V_{SS}$ to V_{DD}	$ I_{IL} $	—	—	0,1	μA
Input voltage LOW	V_{IL}	-0,3	—	+0,8	V
Input voltage HIGH	V_{IH}	2,0	—	$V_{DD}+0,3$	V
Output leakage current at $V_O = V_{SS}$ to V_{DD} ; OD = HIGH or chip disabled	$ I_{OL} $	—	—	0,2	μA
Output voltage LOW at $I_{OL} = 4,0\text{ mA}$	V_{OL}	—	—	0,4	V
Output voltage HIGH at $-I_{OH} = 2,0\text{ mA}$	V_{OH}	2,4	—	—	V

D.C. CHARACTERISTICS ($V_{DD} = 3\text{ V}$) $V_{DD} = 3 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to }+70\text{ }^{\circ}\text{C}$

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	3,0	3,5	V
Operating supply current at $V_I = V_{DD}$ or V_{SS} ; $f = 1\text{ MHz}$; outputs open	I_{DD}	—	5	8	mA
at $V_I = 0,4$ or $1,6\text{ V}$; $f = 1\text{ MHz}$; outputs open	I_{DD}	—	5	8	mA
Standby supply current at $CE2 = V_{SS}$	I_{SB}	—	0,02	5,0	μA
Input leakage current at $V_I = V_{SS}$ to V_{DD}	$ I_{IL} $	—	—	0,1	μA
Input voltage LOW	V_{IL}	-0,3	—	+0,4	V
Input voltage HIGH	V_{IH}	1,6	—	$V_{DD}+0,3$	V
Output leakage current at $V_O = V_{SS}$ to V_{DD} ; OD = HIGH or chip disabled	$ I_{OL} $	—	—	0,2	μA
Output voltage LOW at $I_{OL} = 1,0\text{ mA}$	V_{OL}	—	—	0,3	V
Output voltage HIGH at $-I_{OH} = 1,0\text{ mA}$	V_{OH}	1,7	—	—	V

A.C. TEST CONDITIONS ($V_{DD} = 5\text{ V}$)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load (2 TTL inputs and load capacitance C_L)	Fig. 4

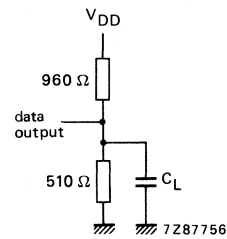


Fig. 4 Test load.

A.C. CHARACTERISTICS ($V_{DD} = 5\text{ V}$)

$V_{DD} = 5 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to }+70\text{ }^{\circ}\text{C}$; loads as per Fig. 4 with $C_L = 100\text{ pF}$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	150	—	—	ns
Address access time	t_{AA}	—	—	150	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	—	—	150	ns
Chip enable CE2 to output	t_{CO2}	—	—	150	ns
Output disable OD to output	t_{OD}	—	—	70	ns
Data output to high impedance state at $C_L = 5\text{ pF}$	t_{DF}	10	—	70	ns
Previously read data valid with respect to address change	t_{OH1}	10	—	—	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	—	—	ns
Write cycle					
Write cycle time	t_{WC}	150	—	—	ns
Write delay time	t_{AW}	0	—	—	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	120	—	—	ns
Chip enable CE2 to write	t_{CW2}	120	—	—	ns
Data set-up time	t_{DW}	70	—	—	ns
Data hold time	t_{DH}	0	—	—	ns
Write pulse duration	t_{WP}	70	—	—	ns
Write recovery time	t_{WR}	0	—	—	ns
Output disable OD set-up time	t_{DS}	70	—	—	ns

A.C. TEST CONDITIONS ($V_{DD} = 3\text{ V}$)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	Fig. 5

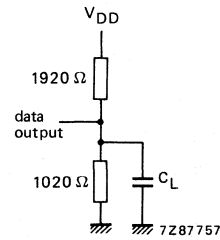


Fig. 5 Test load.

A.C. CHARACTERISTICS ($V_{DD} = 3\text{ V}$)

$V_{DD} = 3 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to }+70\text{ }^{\circ}\text{C}$; loads as per Fig. 5 with $C_L = 100\text{ pF}$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	400	—	—	ns
Address access time	t_{AA}	—	—	400	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	—	—	400	ns
Chip enable CE2 to output	t_{CO2}	—	—	400	ns
Output disable OD to output	t_{OD}	—	—	200	ns
Data output to high impedance state at $C_L = 5\text{ pF}$	t_{DF}	10	—	200	ns
Previously read data valid with respect to address change	t_{OH1}	10	—	—	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	—	—	ns
Write cycle					
Write cycle time	t_{WC}	400	—	—	ns
Write delay time	t_{AW}	0	—	—	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	300	—	—	ns
Chip enable CE2 to write	t_{CW2}	300	—	—	ns
Data set-up time	t_{DW}	200	—	—	ns
Data hold time	t_{DH}	0	—	—	ns
Write pulse duration	t_{WP}	200	—	—	ns
Write recovery time	t_{WR}	0	—	—	ns
Output disable OD set-up time	t_{DS}	200	—	—	ns

WAVEFORMS

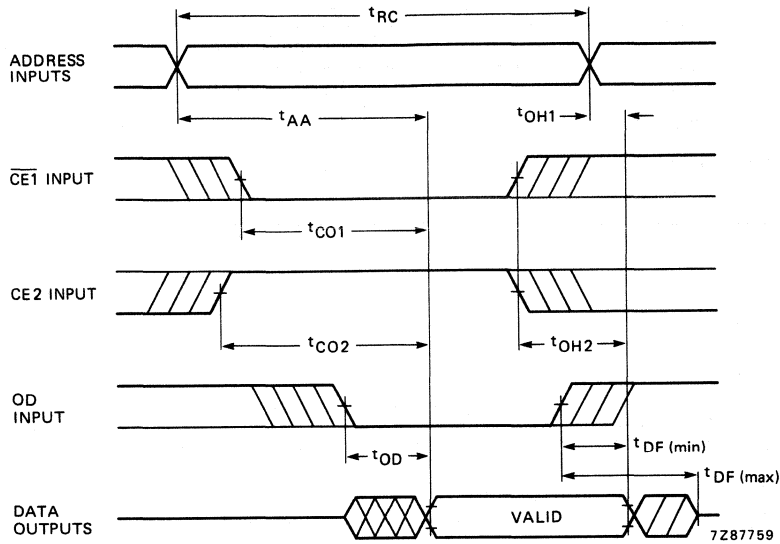


Fig. 6 Read cycle timing; $R/\bar{W} = \text{HIGH}$.

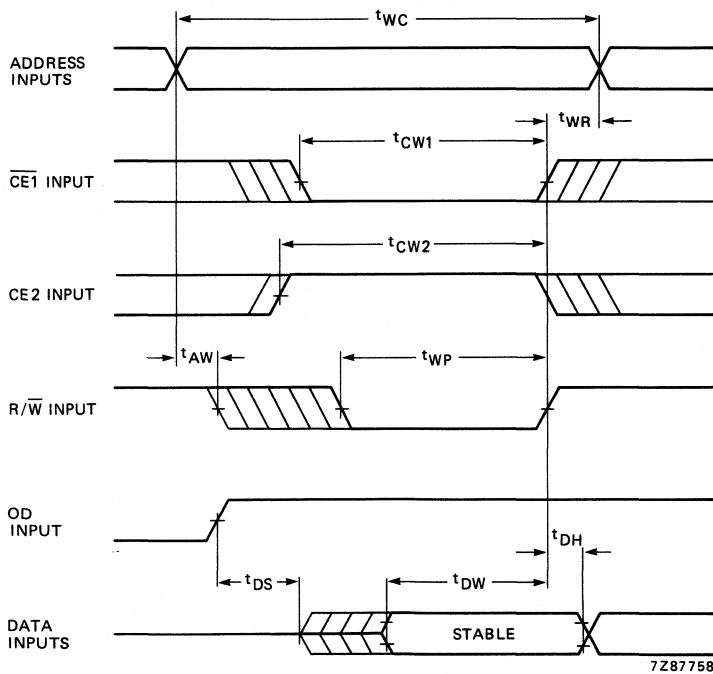


Fig. 7 Write cycle timing.

LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

$CE2 \leq 0,2 \text{ V}$; $T_{amb} = -25 \text{ to } +70 \text{ }^\circ\text{C}$.

parameter	symbol	min.	typ.	max.	unit
Supply voltage for data retention	V_{DR}	1,0	—	5,5	V
Data retention current at $V_{DD} = 1,5 \text{ V}$	I_{DR}	—	0,02	2,0	μA
Chip deselect to data retention time	t_{CDR}	0	—	—	ns
Operation recovery time	t_R	0	—	—	ns

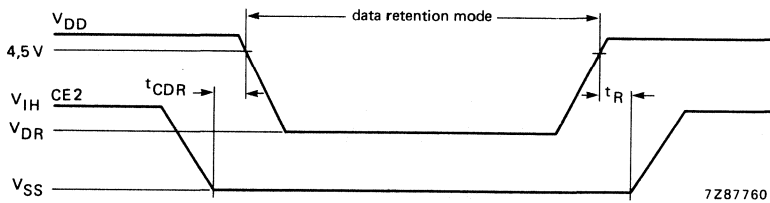


Fig. 8 Low supply voltage data retention characteristics.

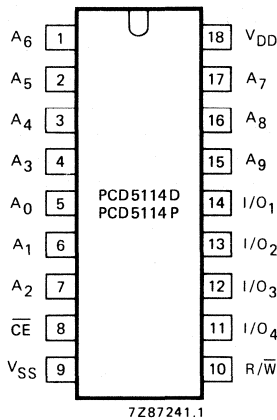


Fig. 2 Pinning diagram: PCD5114D; PCD5114P.

- A₀ to A₃ column address inputs
- A₄ to A₉ row address inputs
- $\overline{\text{CE}}$ chip enable input
- R/ $\overline{\text{W}}$ read/write input

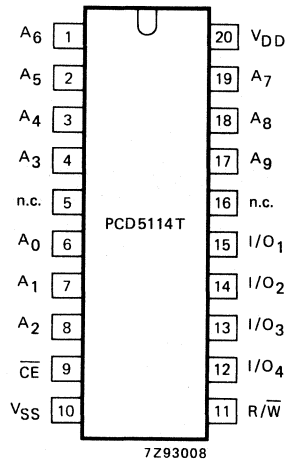


Fig. 3 Pinning diagram: PCD5114T.

- I/O₁ to I/O₄ data input/output
- V_{SS} negative supply (ground)
- V_{DD} positive supply (+ 5 V)

Table 1 Mode selection

$\overline{\text{CE}}$	R/ $\overline{\text{W}}$	mode	output	power
H	H	not selected	high impedance	standby
H	L	not selected	high impedance	standby
L	H	read	active	active
L	L	write	high impedance	active

H = HIGH logic level (the most positive voltage)

L = LOW logic level (the most negative voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V _{DD}	-0,3 to + 8 V
Input voltage range (any pin)	V _I	V _{SS} -0,3 to V _{DD} + 0,3 V
Storage temperature range	T _{stg}	-55 to + 125 °C
Operating ambient temperature range	T _{amb}	-25 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

D.C. CHARACTERISTICS
 $V_{DD} = 5 \text{ V} \pm 0,5 \text{ V}$; $V_{SS} = 0 \text{ V}$; $T_{amb} = -25 \text{ to } +70 \text{ }^{\circ}\text{C}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; $f = 1 \text{ MHz}$; outputs open	I_{DD}	—	10	17	mA
at $V_I = 0,8 \text{ V}/2,0 \text{ V}$; $f = 1 \text{ MHz}$; outputs open	I_{DD}	—	10	17	mA
at $V_I = 0,8 \text{ V}/2,0 \text{ V}$; $f = 5 \text{ MHz}$; outputs open	I_{DD}	—	12	20	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	—	0,02	5	μA
Input voltage HIGH	V_{IH}	2,0	—	$V_{DD} + 0,3$	V
Input voltage LOW	V_{IL}	-0,3	—	+0,8	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	—	—	0,1	μA
Output voltage HIGH					
at $-I_{OH} = 2 \text{ mA}$	V_{OH}	2,4	—	—	V
Output voltage LOW					
at $I_{OL} = 4 \text{ mA}$	V_{OL}	—	—	0,4	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD} ; $\overline{CE} = \text{HIGH}$	$\pm I_{OL}$	—	—	0,5	μA

D.C. CHARACTERISTICS
 $V_{DD} = 3 \text{ V} \pm 0,5 \text{ V}$; $V_{SS} = 0 \text{ V}$; $T_{amb} = -25 \text{ to } +70 \text{ }^{\circ}\text{C}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; $f = 1 \text{ MHz}$; outputs open	I_{DD}	—	5	8	mA
at $V_I = 0,4 \text{ V}/1,6 \text{ V}$; $f = 1 \text{ MHz}$; outputs open	I_{DD}	—	5	8	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	—	0,02	5	μA
Input voltage HIGH	V_{IH}	1,6	—	$V_{DD} + 0,3$	V
Input voltage LOW	V_{IL}	-0,3	—	+0,4	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	—	—	0,1	μA
Output voltage HIGH					
at $-I_{OH} = 1 \text{ mA}$	V_{OH}	1,7	—	—	V
Output voltage LOW					
at $I_{OL} = 1 \text{ mA}$	V_{OL}	—	—	0,3	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD} ; $\overline{CE} = \text{HIGH}$	$\pm I_{OL}$	—	—	0,5	μA

DEVELOPMENT DATA

A.C. CHARACTERISTICS

$V_{DD} = 5 \text{ V} \pm 0,5 \text{ V}$; $V_{SS} = 0 \text{ V}$; $T_{amb} = -25 \text{ to } +70 \text{ }^\circ\text{C}$; measured in Fig. 4, $C_L = 100 \text{ pF}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	200	—	—	ns
Address access time	t_{AA}	—	—	200	ns
Chip select access time	t_{AC}	—	—	200	ns
Output hold from address change	t_{OHA}	20	—	—	ns
Output hold from chip select	t_{OHC}	20	—	—	ns
Output to low impedance from chip selection at $C_L = 5 \text{ pF}$	t_{CLZ}	20	—	—	ns
Output to high impedance from chip deselection at $C_L = 5 \text{ pF}$	t_{CHZ}	—	—	80	ns
Write cycle					
Write cycle time	t_{WC}	200	—	—	ns
Chip selection to end of write	t_{CW}	120	—	—	ns
Address set-up time	t_{AS}	0	—	—	ns
Write pulse duration	t_{WP}	140	—	—	ns
Write recovery time	t_{WR}	0	—	—	ns
Data set-up time	t_{DS}	80	—	—	ns
Data hold time	t_{DH}	0	—	—	ns
Output to high impedance from write enabled at $C_L = 5 \text{ pF}$	t_{WZ}	—	—	60	ns
Output active from end of write at $C_L = 5 \text{ pF}$	t_{RZ}	20	—	—	ns

A.C. TEST CONDITIONS (see Fig. 4)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load	2 TTL gates and $C_L = 100 \text{ pF}$

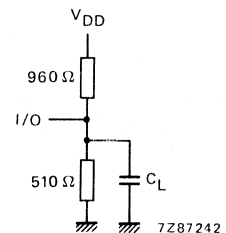


Fig. 4 Load for a.c. test conditions ($V_{DD} = 5 \text{ V} \pm 0,5 \text{ V}$).

A.C. CHARACTERISTICS

$V_{DD} = 3\text{ V} \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to } +70^{\circ}\text{C}$; measured in Fig. 5, $C_L = 100\text{ pF}$; unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t _{RC}	500	—	—	ns
Address access time	t _{AA}	—	—	500	ns
Chip select access time	t _{AC}	—	—	500	ns
Output hold from address change	t _{OHA}	20	—	—	ns
Output hold from chip select	t _{OHC}	20	—	—	ns
Output to low impedance from chip selection at $C_L = 5\text{ pF}$	t _{CLZ}	20	—	—	ns
Output to high impedance from chip deselection at $C_L = 5\text{ pF}$	t _{CHZ}	—	—	200	ns
Write cycle					
Write cycle time	t _{WC}	500	—	—	ns
Chip selection to end of write	t _{CW}	300	—	—	ns
Adres set-up time	t _{AS}	0	—	—	ns
Write pulse duration	t _{WP}	350	—	—	ns
Write recovery time	t _{WR}	0	—	—	ns
Data set-up time	t _{DS}	200	—	—	ns
Data hold time	t _{DH}	0	—	—	ns
Output to high impedance from write enabled at $C_L = 5\text{ pF}$	t _{WZ}	—	—	150	ns
Output active from end of write at $C_L = 5\text{ pF}$	t _{RZ}	20	—	—	ns

A.C. TEST CONDITIONS (see Fig. 5)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	2 TTL gates and $C_L = 100\text{ pF}$

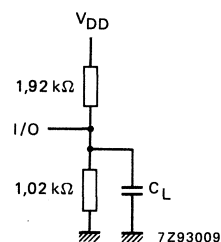


Fig. 5 Load for a.c. test conditions ($V_{DD} = 3\text{ V} \pm 0,5\text{ V}$).

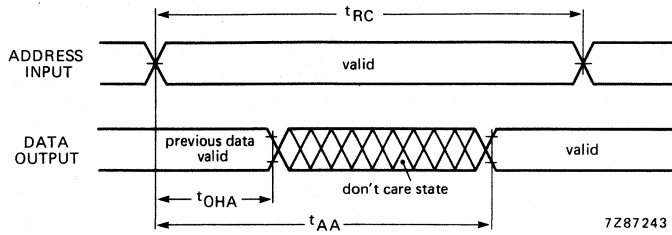


Fig. 6 Read cycle timing (1): $\overline{R/\overline{W}}$ is HIGH; \overline{CE} is LOW for a read cycle.

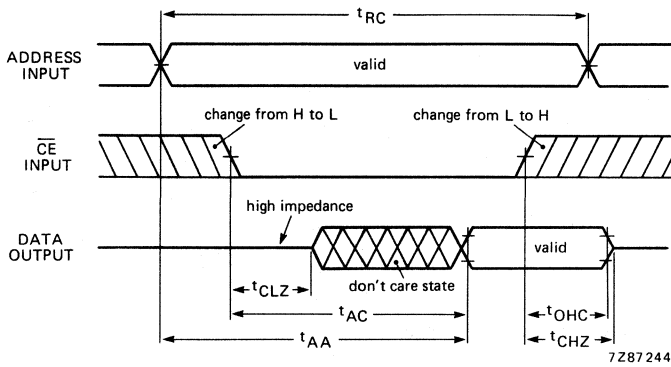


Fig. 7 Read cycle timing (2): $\overline{R/\overline{W}}$ is HIGH for a read cycle.

DEVELOPMENT DATA

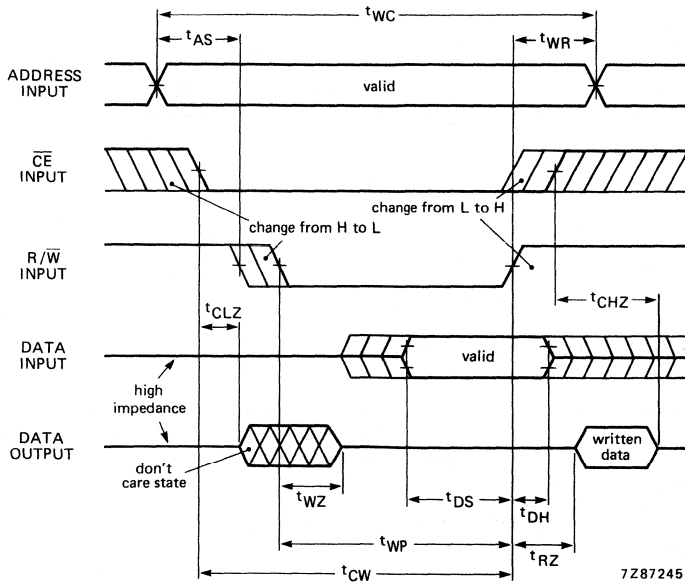


Fig. 8 Write cycle (1): R/W controlled.

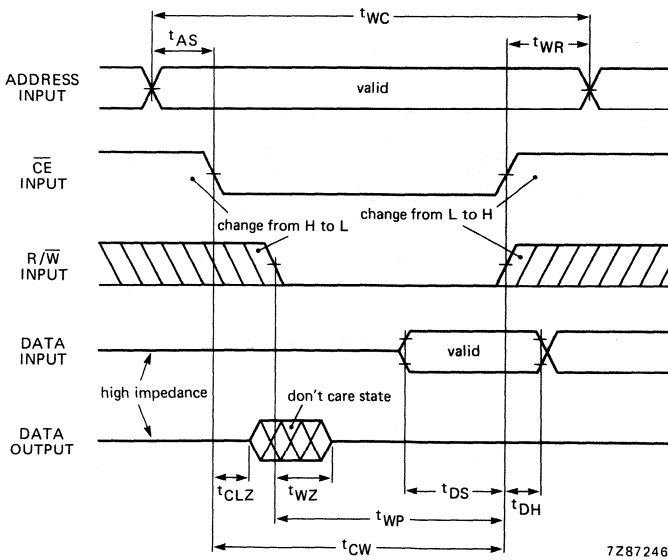


Fig. 9 Write cycle (2): CE controlled.

Note : If the CE low transition occurs after the R/W low transition, the outputs remain in the high impedance state.

CAPACITANCE

$f = 1 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$

parameter	symbol	min.	typ.	max.	unit
Input capacitance at $V_I = V_{SS}$	C_I	—	—	5	pF
Output capacitance at $V_O = V_{SS}$	C_O	—	—	5	pF

LOW V_{DD} DATA RETENTION CHARACTERISTICS

$T_{\text{amb}} = -25 \text{ to } +70 \text{ }^{\circ}\text{C}$

parameter	symbol	min.	typ.	max.	unit
V_{DD} for data retention at $\overline{CE} = V_{DDR} \pm 0,2 \text{ V}; V_I = V_{DDR} \text{ to } V_{SS}$	V_{DDR}	1	—	5,5	V
Data retention current at $V_{DDR} = 1,5 \text{ V}$	I_{DDR}	—	0,02	2	μA
Chip deselect to data retention time	t_{CR}	0	—	—	ns
Operation recovery time	t_R	0	—	—	ns

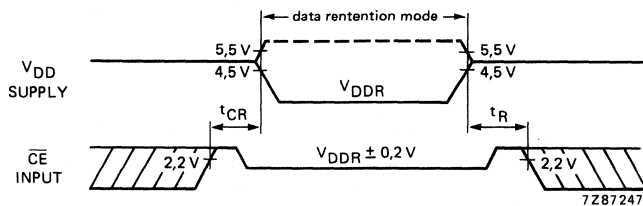


Fig. 10 LOW V_{DD} data retention.

256 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μ A
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications) channel presets
- Radio and television
- Video cassette recorder
- General purpose RAM expansion for the microcontroller families MAB8400 and PCF84C00

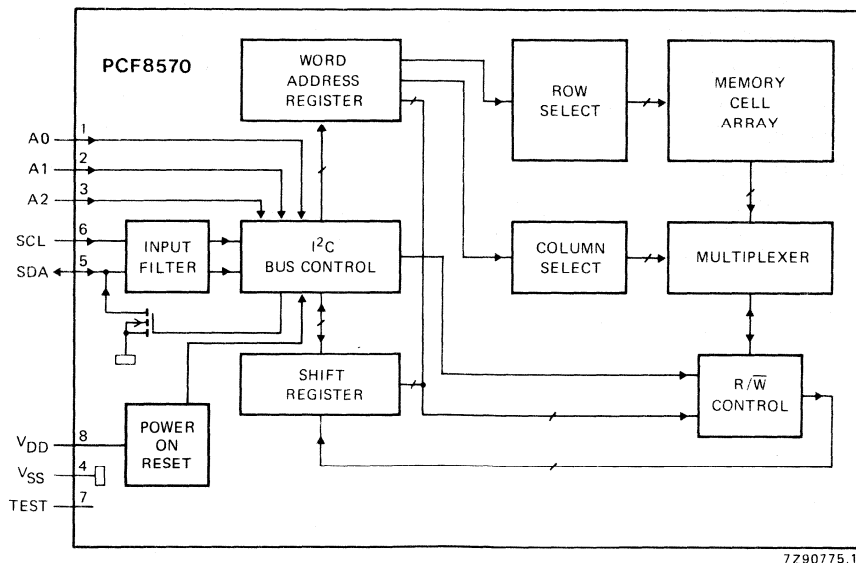


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8570P: 8-lead DIL; plastic (SOT-97AE).

PCF8570T: 8-lead mini-pack plastic (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V _{SS}	negative supply
5	SDA	serial data line
6	SCL	serial clock line
7	TEST	test input for test speed-up; must be connected to V _{SS} when not in use (power saving mode, see Figs 14 and 15)
8	V _{DD}	

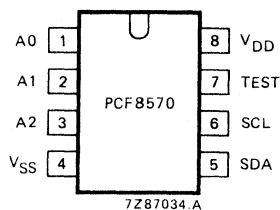


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V _{DD}	-0,8 to + 8,0 V
Voltage range on any input	V _I	-0,8 to V _{DD} + 0,8 V
D.C. input current (any input)	± I _I	max. 10 mA
D.C. output current (any output)	± I _O	max. 10 mA
Supply current (pin 4 or pin 8)	± I _{DD} ; I _{SS}	max. 50 mA
Power dissipation per package	P _{tot}	max. 300 mW
Power dissipation per output	P	max. 50 mW
Storage temperature range	T _{stg}	-65 to + 150 °C
Operating ambient temperature range	T _{amb}	-40 to + 85 °C

CHARACTERISTICS

 $V_{DD} = 2,5$ to 6 V; $V_{SS} = 0$ V; $T_{amb} = -40$ to $+85$ °C unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	—	6	V
Supply current at $V_I = V_{SS}$ or V_{DD} operating at $f_{SCL} = 100$ kHz	I_{DD}	—	—	200	μ A
standby at $f_{SCL} = 0$ Hz	I_{DDO}	—	—	15	μ A
standby at $T_{amb} = -25$ to $+70$ °C	I_{DDO}	—	—	5	μ A
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	-0,8	—	$0,3 \times V_{DD}$	V
Input voltage HIGH**	V_{IH}	$0,7 \times V_{DD}$	—	$V_{DD} + 0,8$	V
Output current LOW at $V_{OL} = 0,4$ V	I_{OL}	3	—	—	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	—	—	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	—	—	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	—	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	—	—	7	pF
Tolerable spike width on bus	t_{SW}	—	—	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	—	6	V
Supply current at $V_{DDR} = 1$ V	I_{DDR}	—	—	5	μ A
Supply current at $V_{DDR} = 1$ V; $T_{amb} = -25$ to $+70$ °C	I_{DDR}	—	—	2	μ A
Power saving mode (Figs 14 and 15)					
Supply current at $T_{amb} = 25$ °C; TEST = V_{DDR}	I_{DDR}	—	50	400	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed $\pm 0,5$ mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

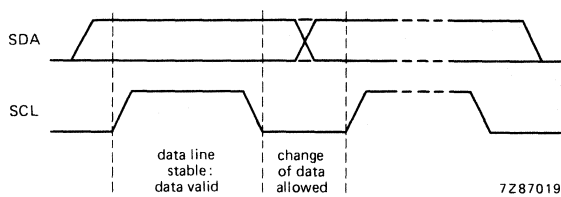


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

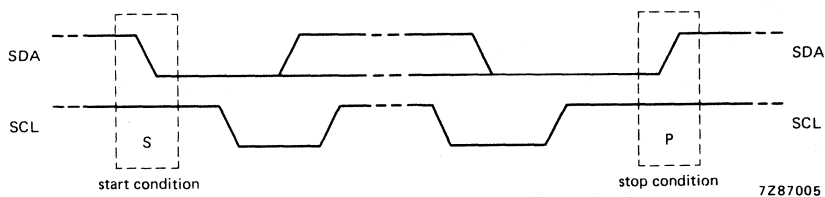


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

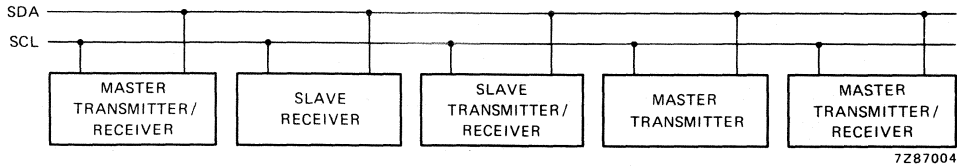


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

DEVELOPMENT DATA

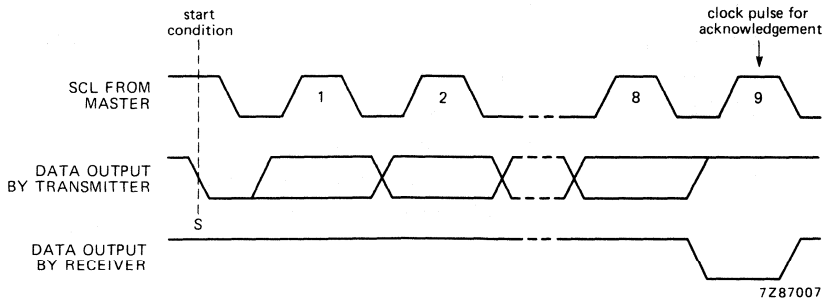


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

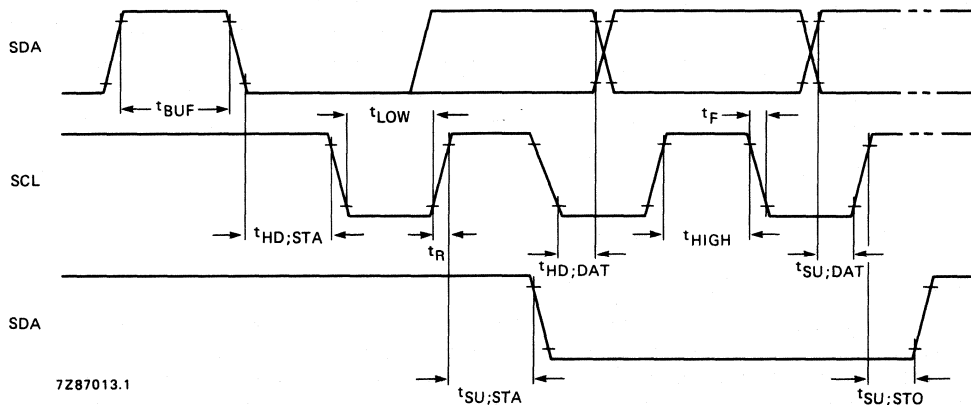


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD; STA}$	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU; STA}$	$t \geq t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD; DAT}$	$t \geq 0 \mu s$	Data hold time
$t_{SU; DAT}$	$t \geq 250 ns$	Data set-up time
t_R	$t \leq 1 \mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300 ns$	Fall time of both the SDA and SCL line
$t_{SU; STO}$	$t \geq t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD} .

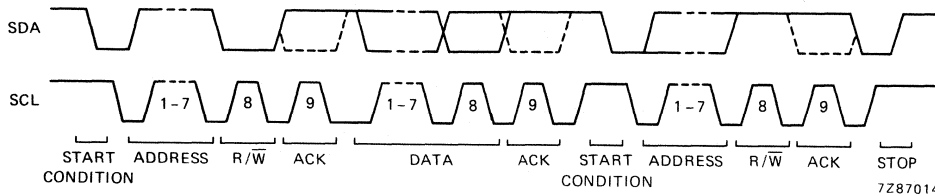


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin} 4,7 μs

$t_{HIGHmin}$ 4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio 1 : 1 (LOW-to-HIGH)

Max. number of bytes unrestricted

Premature termination of transfer allowed by generation of STOP condition

Acknowledge clock bit must be provided by the master

DEVELOPMENT DATA

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs . The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

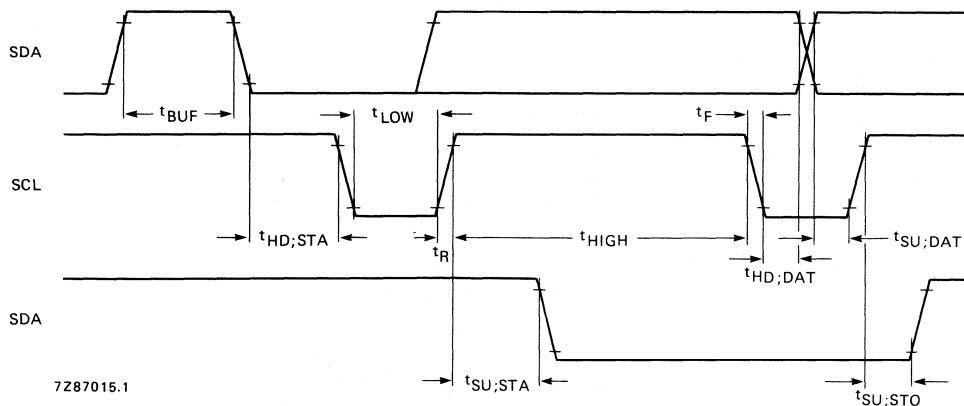


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geq 105 \mu\text{s}$ (t_{LOWmin})
$t_{\text{HD; STA}}$	$t \geq 365 \mu\text{s}$ (t_{HIGHmin})
t_{LOW}	$130 \mu\text{s} \pm 25 \mu\text{s}$
t_{HIGH}	$390 \mu\text{s} \pm 25 \mu\text{s}$
$t_{\text{SU; STA}}$	$130 \mu\text{s} \pm 25 \mu\text{s}^*$
$t_{\text{HD; DAT}}$	$t \geq 0 \mu\text{s}$
$t_{\text{SU; DAT}}$	$t \geq 250 \text{ ns}$
t_{R}	$t \leq 1 \mu\text{s}$
t_{F}	$t \leq 300 \text{ ns}$
$t_{\text{SU; STO}}$	$130 \mu\text{s} \pm 25 \mu\text{s}$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD} . For definitions see high-speed mode.

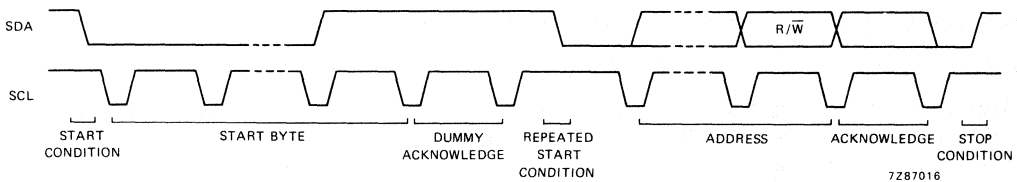


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130 \mu\text{s} \pm 25 \mu\text{s}$
t_{HIGHmin}	$390 \mu\text{s} \pm 25 \mu\text{s}$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570 READ and WRITE cycles is shown in Fig. 11.

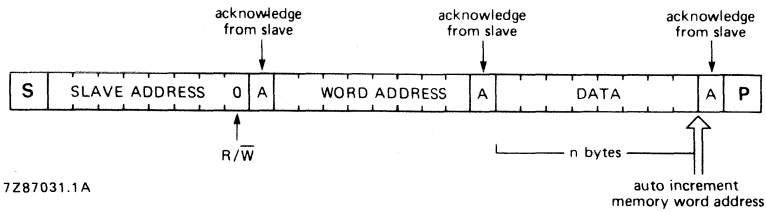


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

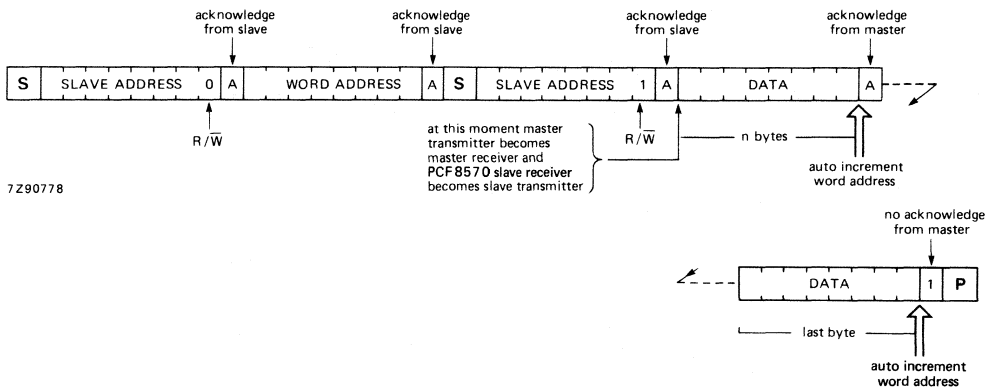


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

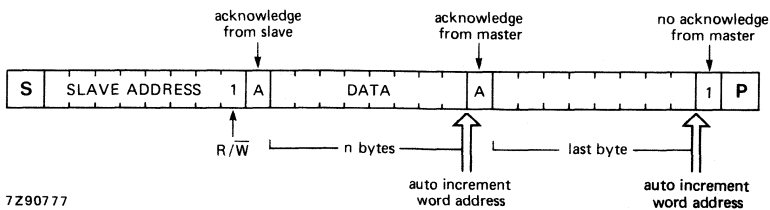


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

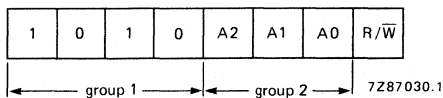


Fig. 12 PCF8570 address.

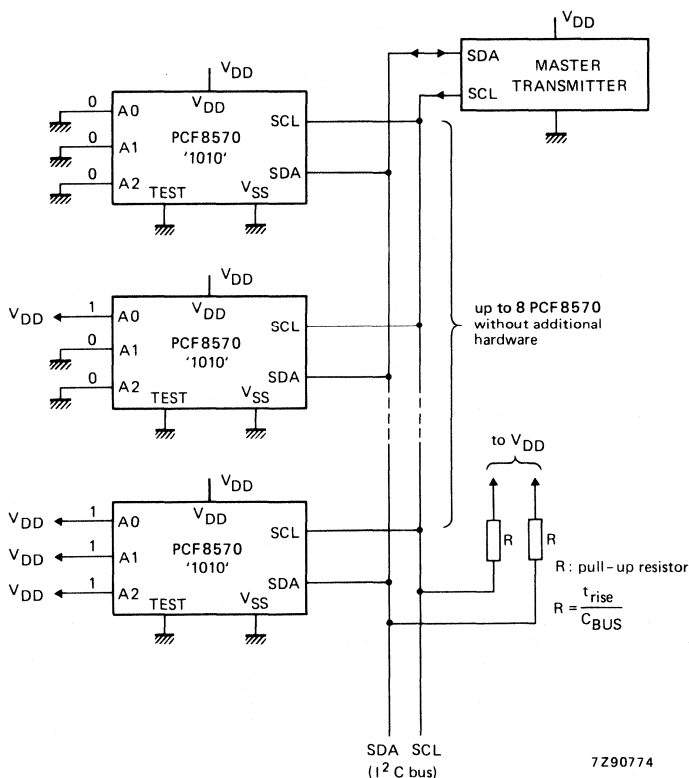


Fig. 13 PCF8570 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition $TEST = V_{DDR}$, the PCF8570 goes into the power saving mode and the I²C bus logic is reset.

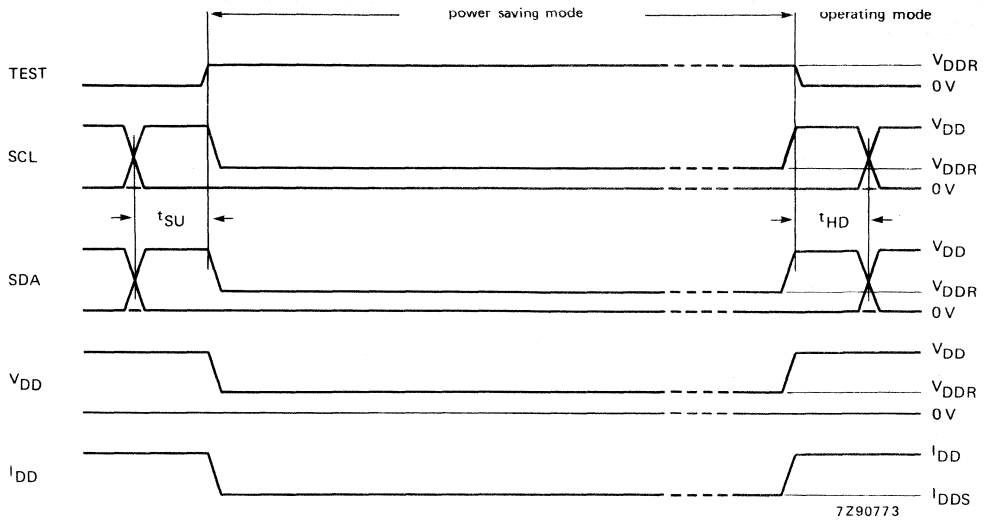


Fig. 14 Timing for power saving mode.

Where:

$t_{SU} \geq 4 \mu s$

$t_{HD} \geq 4 \mu s$

DEVELOPMENT DATA

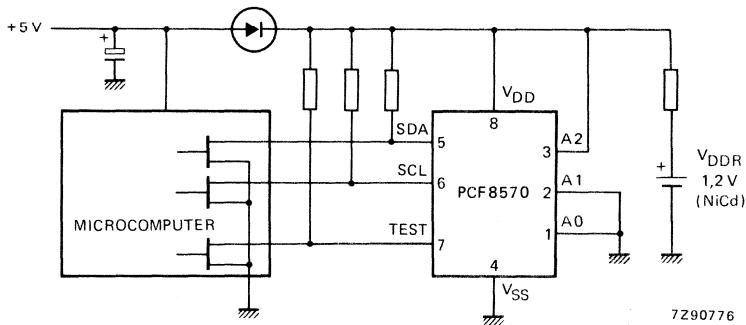
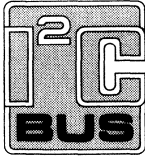


Fig. 15 Application example for power saving mode.

Note to Fig. 15

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

128 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 μ A
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony RAM expansion for stored numbers in repertory dialling (e.g. PCD3340 applications) channel presets
- Radio and television
- Video cassette recorder
- General purpose RAM expansion for the microcomputer families MAB8400 and PCF84C00

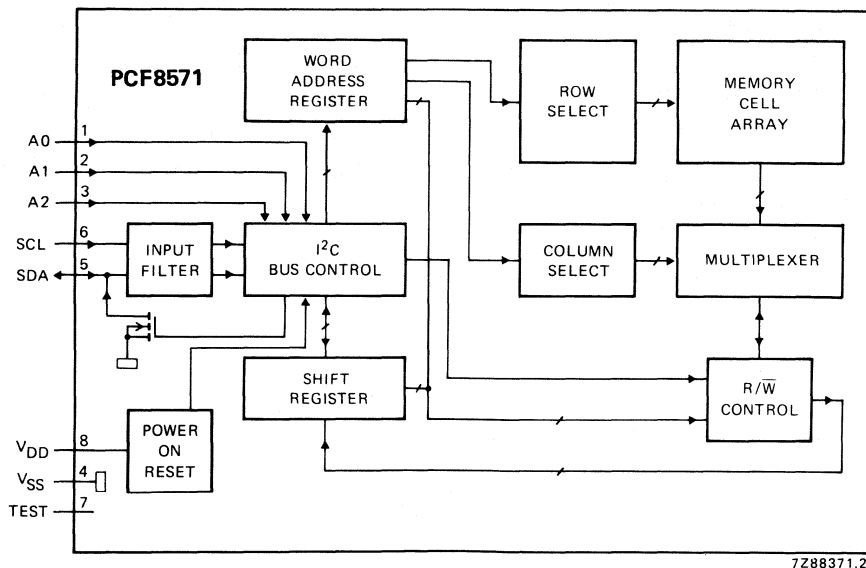


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8571P : 8-lead DIL; plastic (SOT-97AE).
 PCF8571T : 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs	
4	V _{SS}	negative supply	
5	SDA	serial data line	} I ² C bus
6	SCL	serial clock line	
7	TEST	test input for test speed-up; must be connected to V _{SS} when not in use (power saving mode, see Fig. 14 and 15)	
8	V _{DD}	positive supply	

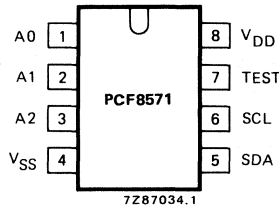


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V _{DD}		-0,8 to + 8,0 V
Voltage range on any input	V _I		-0,8 to V _{DD} + 0,8 V
D.C. input current (any input)	± I _I	max.	10 mA
D.C. output current (any output)	± I _O	max.	10 mA
Supply current (pin 4 or pin 8)	± I _{DD} ; I _{SS}	max.	50 mA
Power dissipation per package	P _{tot}	max.	300 mW
Power dissipation per output	P	max.	50 mW
Storage temperature range	T _{stg}		-65 to + 150 °C
Operating temperature range	T _{amb}		-40 to + 85 °C

CHARACTERISTICS

 $V_{DD} = 2,5$ to 6 V; $V_{SS} = 0$ V; $T_{amb} = -40$ to $+85$ °C unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage	V_{DD}	2,5	—	6	V
Supply current					
$V_I = V_{SS}$ or V_{DD}					
operating at $f_{SCL} = 100$ kHz;	I_{DD}	—	—	200	μ A
standby at $f_{SCL} = 0$ Hz	I_{DDO}	—	—	15	μ A
standby at $T_{amb} = -25$ to 70 °C	I_{DDO}	—	—	5	μ A
Power-on reset voltage level at $V_{SCL} = V_{SDA} = V_{DD}$	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	-0,8	—	$0,3 \times V_{DD}$	V
Input voltage HIGH**	V_{IH}	$0,7 \times V_{DD}$	—	$V_{DD} + 0,8$	V
Output current LOW at $V_{OL} = 0,4$ V	I_{OL}	3	—	—	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	—	—	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	—	—	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	—	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	—	—	7	pF
Tolerable spike width on bus	t_{SW}	—	—	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	—	6	V
Supply current at $V_{DDR} = 1$ V	I_{DDR}	—	—	5	μ A
Supply current at $V_{DDR} = 1$ V; $T_{amb} = -25$ to 70 °C	I_{DDR}	—	—	2	μ A
Power saving mode (Fig. 14)					
Supply current at $T_{amb} = 25$ °C; TEST = V_{DDR}	I_{DDS}	—	50	200	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed $\pm 0,5$ mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

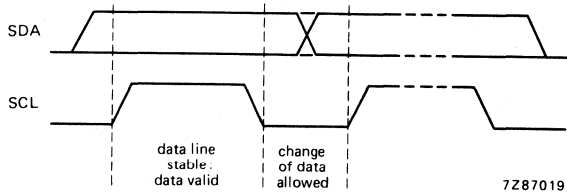


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

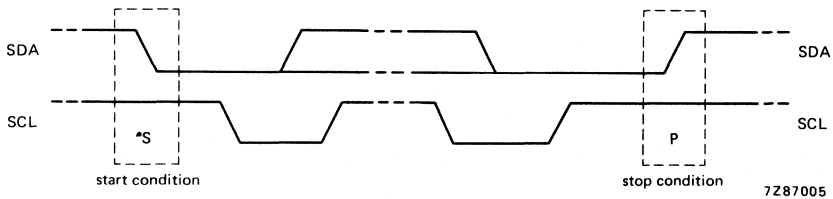


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

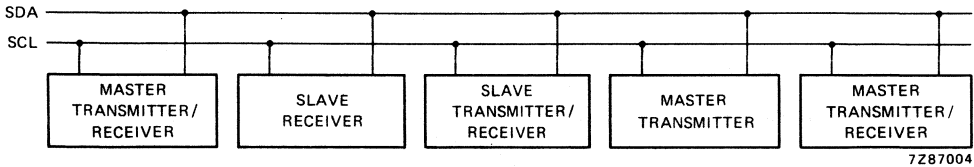


Fig. 5 System configuration.

Acknowledge

DEVELOPMENT DATA

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

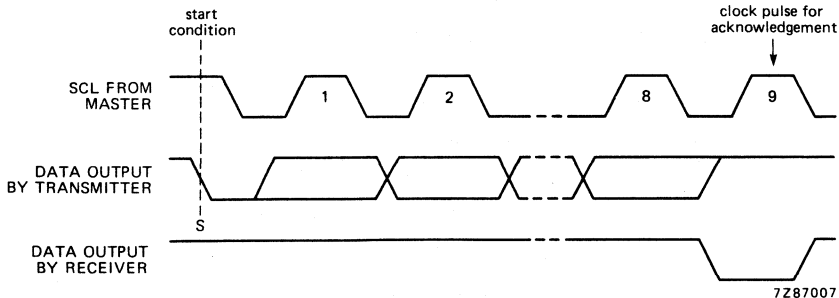


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8571 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

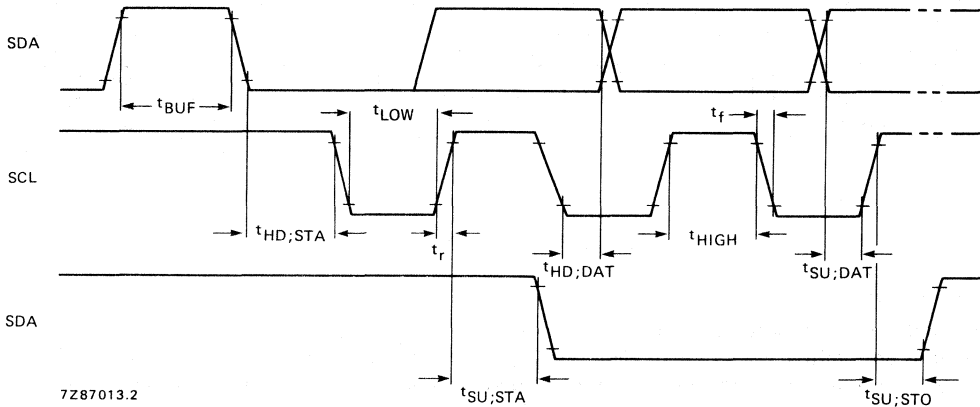


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD; STA}$	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	$4,7 \mu s$	Clock LOW period
$t_{HIGHmin}$	$4 \mu s$	Clock HIGH period
$t_{SU; STA}$	$t \geq t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD; DAT}$	$t \geq 0 \mu s$	Data hold time
$t_{SU; DAT}$	$t \geq 250 ns$	Data set-up time
t_r	$t \leq 1 \mu s$	Rise time of both the SDA and SCL line
t_f	$t \leq 300 ns$	Fall time of both the SDA and SCL line
$t_{SU; STO}$	$t \geq t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD} .

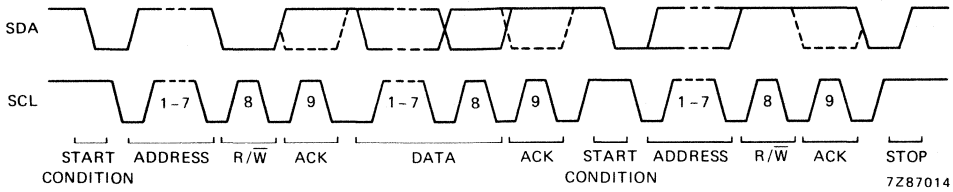


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin} 4,7 μs

$t_{HIGHmin}$ 4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio 1 : 1 (LOW-to-HIGH)

Max. number of bytes unrestricted

Premature termination of transfer allowed by generation of STOP condition

Acknowledge clock bit must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs . The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

DEVELOPMENT DATA

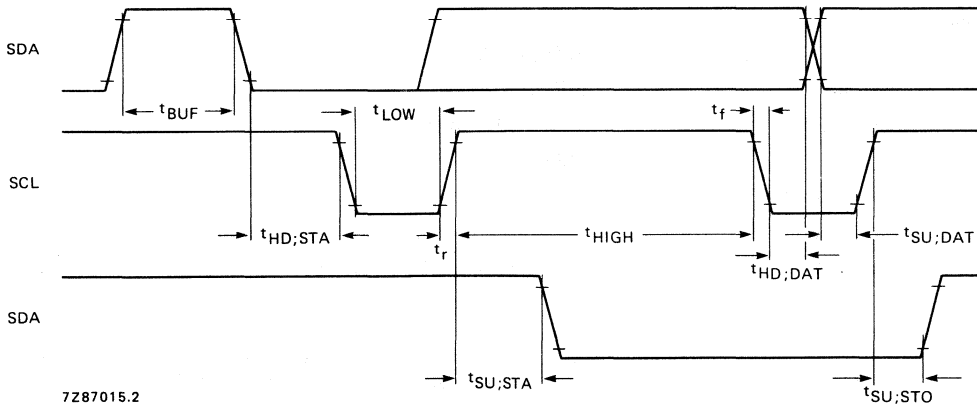


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t _{BUF}	$t \geq 105 \mu\text{s}$ (t _{LOWmin})
t _{HD; STA}	$t \geq 365 \mu\text{s}$ (t _{HIGHmin})
t _{LOW}	$130 \mu\text{s} \pm 25 \mu\text{s}$
t _{HIGH}	$390 \mu\text{s} \pm 25 \mu\text{s}$
t _{SU; STA}	$130 \mu\text{s} \pm 25 \mu\text{s}^*$
t _{HD; DAT}	$t \geq 0 \mu\text{s}$
t _{SU; DAT}	$t \geq 250 \text{ ns}$
t _r	$t \leq 1 \mu\text{s}$
t _f	$t \leq 300 \text{ ns}$
t _{SU; STO}	$130 \mu\text{s} \pm 25 \mu\text{s}$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

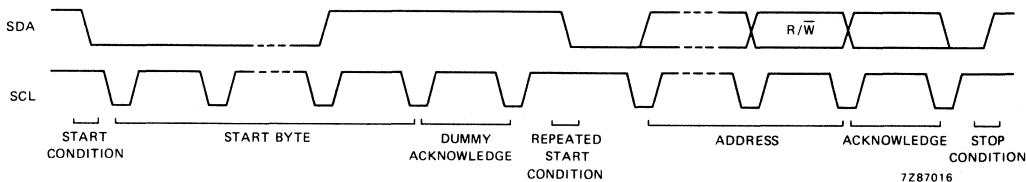


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t _{LOWmin}	$130 \mu\text{s} \pm 25 \mu\text{s}$
t _{HIGHmin}	$390 \mu\text{s} \pm 25 \mu\text{s}$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8571 READ and WRITE cycles is shown in Fig. 11.

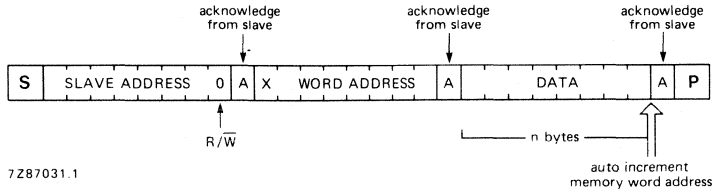


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

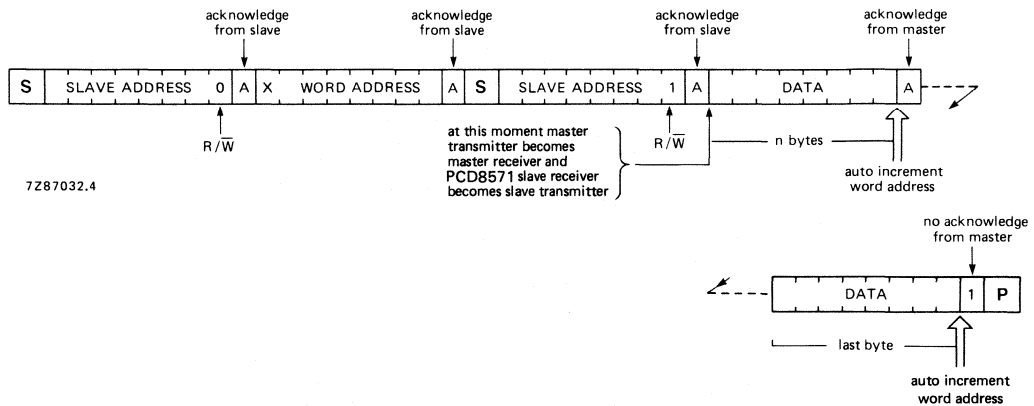


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

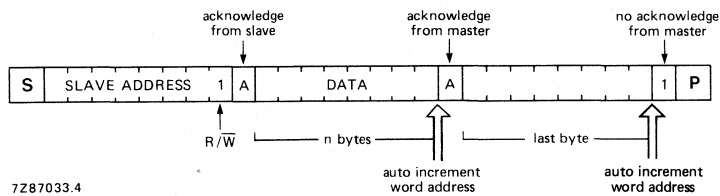


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

Note

X = don't care bit.

DEVELOPMENT DATA

APPLICATION INFORMATION

The PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

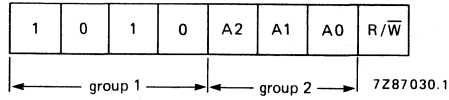


Fig. 12 PCF8571 address.

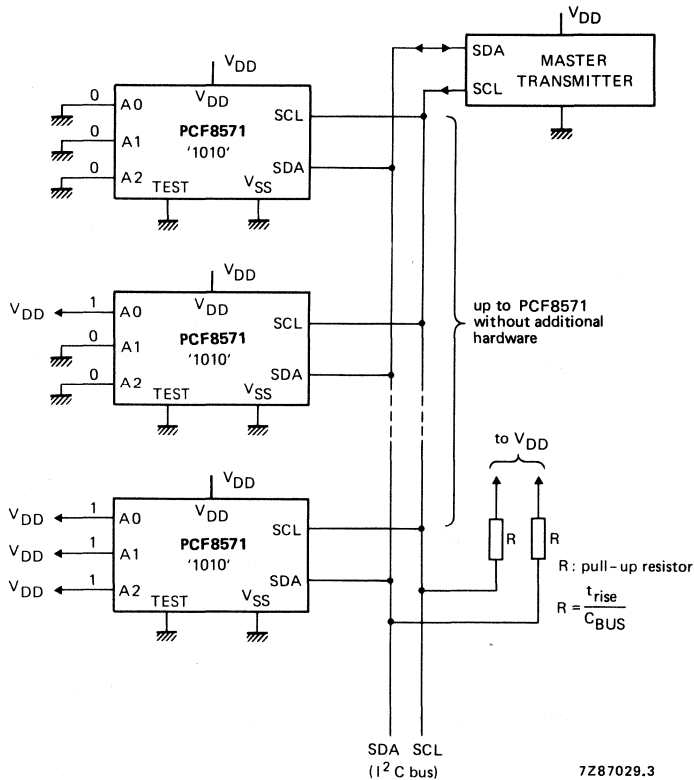


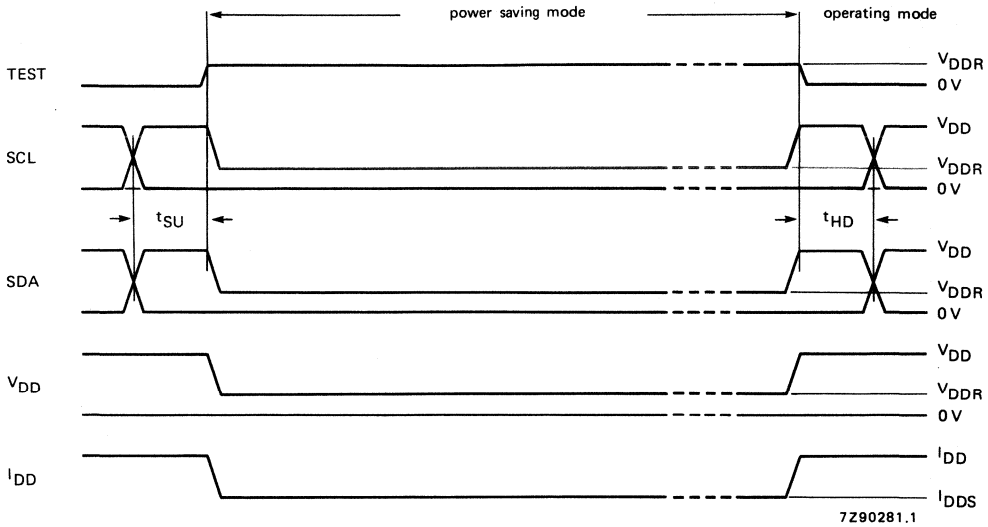
Fig. 13 PCF8571 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition $TEST = V_{DDR}$, the PCF8571 goes into the power saving mode and I²C bus logic is reset.



DEVELOPMENT DATA

Where:
 $t_{SU} \geq 4 \mu s$
 $t_{HD} \geq 4 \mu s$

Fig. 14 Timing for power saving mode.

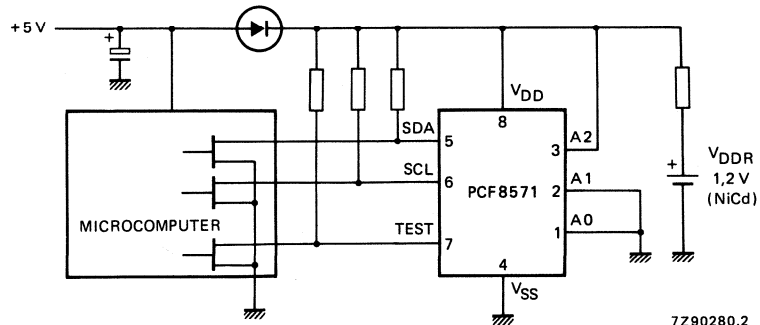


Fig. 15 Application example for power saving mode.

Note

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.



256 x 8-BIT STATIC RAM WITH ALARM CLOCK/CALENDAR AND BCD-COUNTER

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C bus interface operating supply voltage: 2,5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1,0 V to 6 V
- Data retention voltage: 1,0 V to 6 V
- Low standby current: max. 15 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

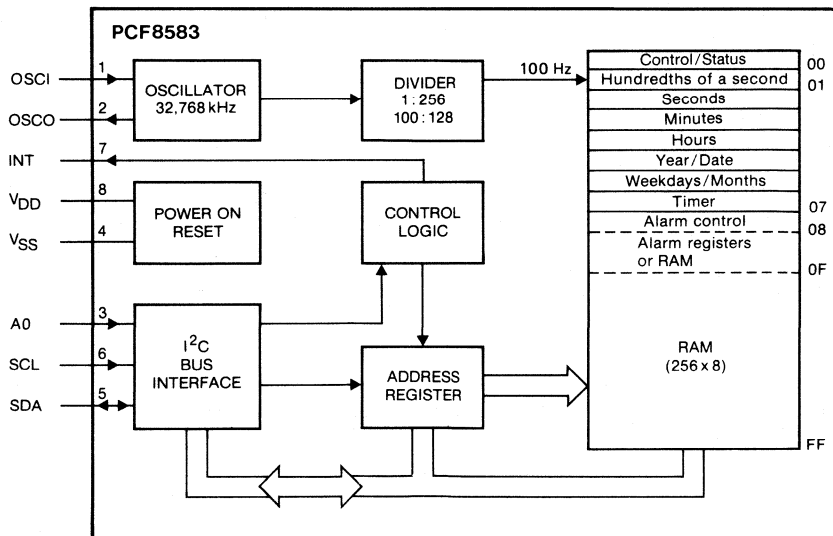


Fig. 1 Block diagram.

7Z81191.1

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT-97AE).

PCF8583T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input
2	OSCO	oscillator output
3	A0	address input
4	V _{SS}	negative supply
5	SDA	} I ² C bus
6	SCL	
7	INT	open drain interrupt output (active low)
8	V _{DD}	positive supply

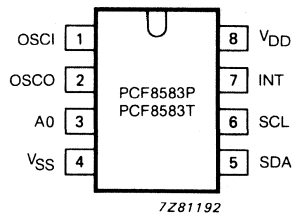


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8); note 1	V _{DD}	-0,8 to 8,0 V
Voltage range on any input	V _I	-0,8 to V _{DD} + 0,8 V
D.C. input current (any input)	I _I	max. 10 mA
D.C. output current (any output)	I _O	max. 10 mA
Supply current (pin 4 or pin 8)	I _{DD} ; I _{SS}	max. 50 mA
Power dissipation per package	P _{tot}	max. 300 mW
Power dissipation per output	P	max. 50 mW
Storage temperature range	T _{stg}	-65 to + 150 °C
Operating ambient temperature range	T _{amb}	-40 to + 85 °C

Note

- Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I²C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32,768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

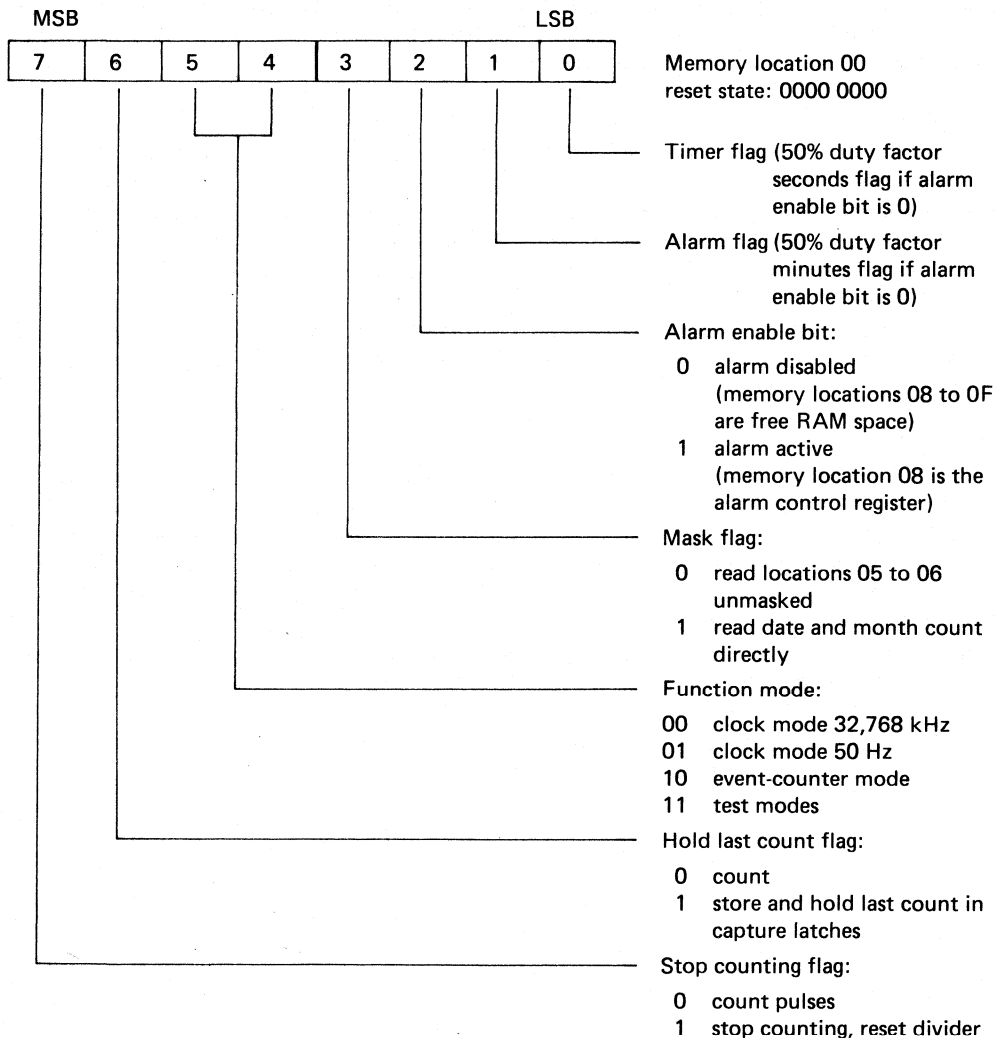


Fig. 3 Control/status register.

Counter registers

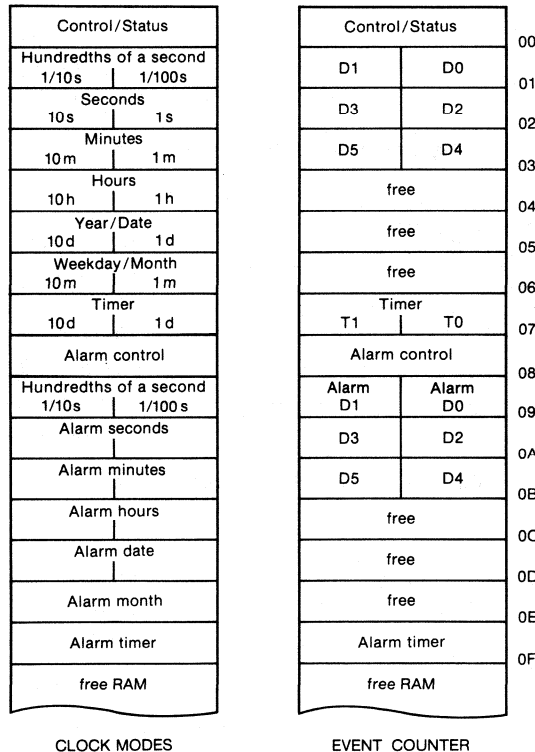
In the different modes the counter registers are programmed and arranged as shown in Fig. 4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig. 5.

The year and date are packed into memory location 05 (see Fig. 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

DEVELOPMENT DATA



7281195

Fig. 4 Register arrangement.

Counter registers (continued)

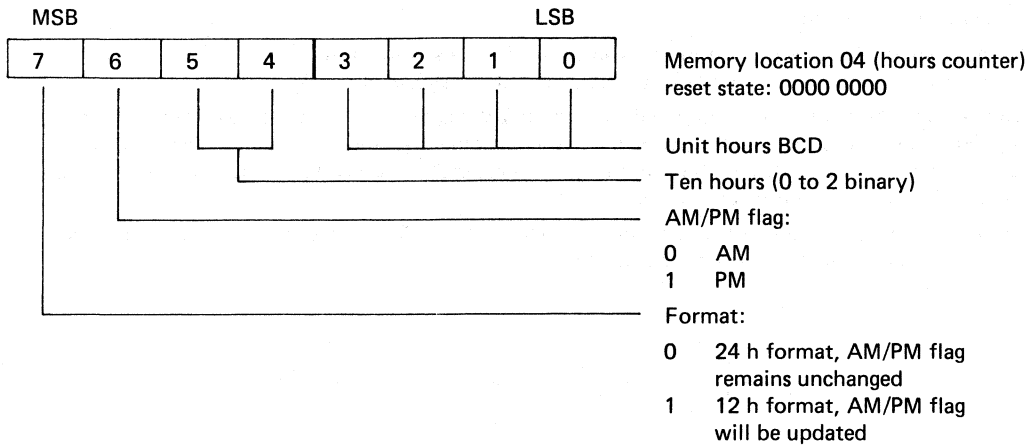


Fig. 5 Format of the hours counter.

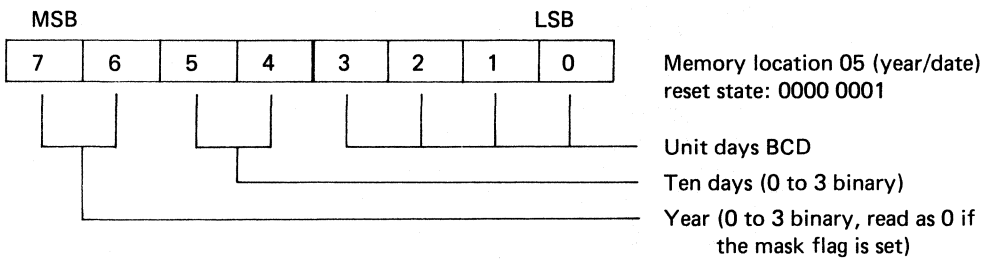


Fig. 6 Format of the year/date counter.

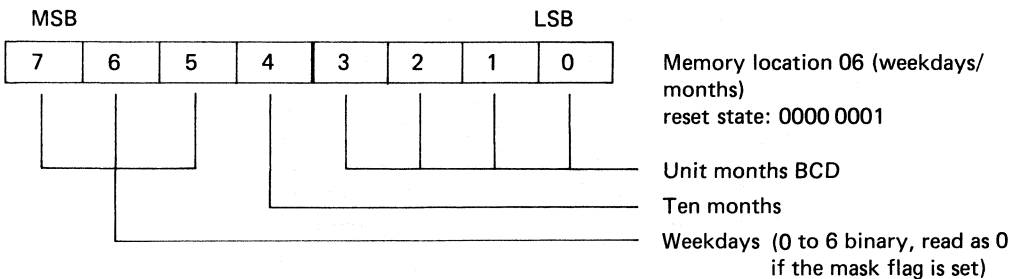


Fig. 7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, 12
	01 to 30	30 to 01	4, 6, 9, 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer/days	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

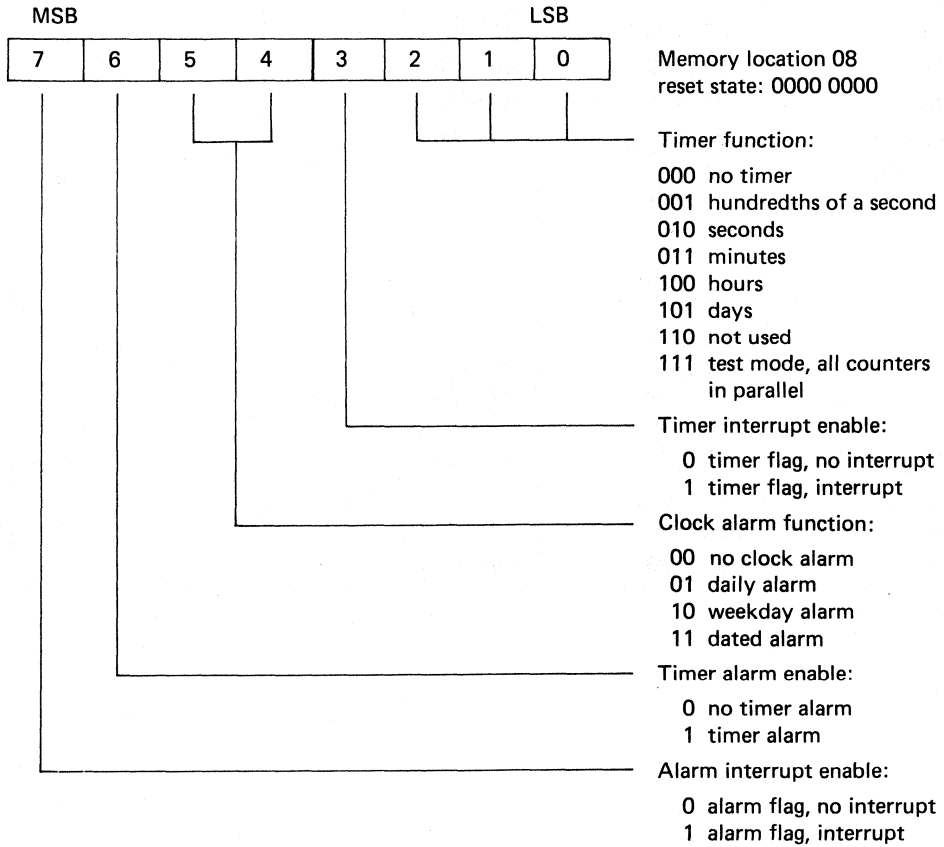


Fig. 8a Alarm control register, clock modes.

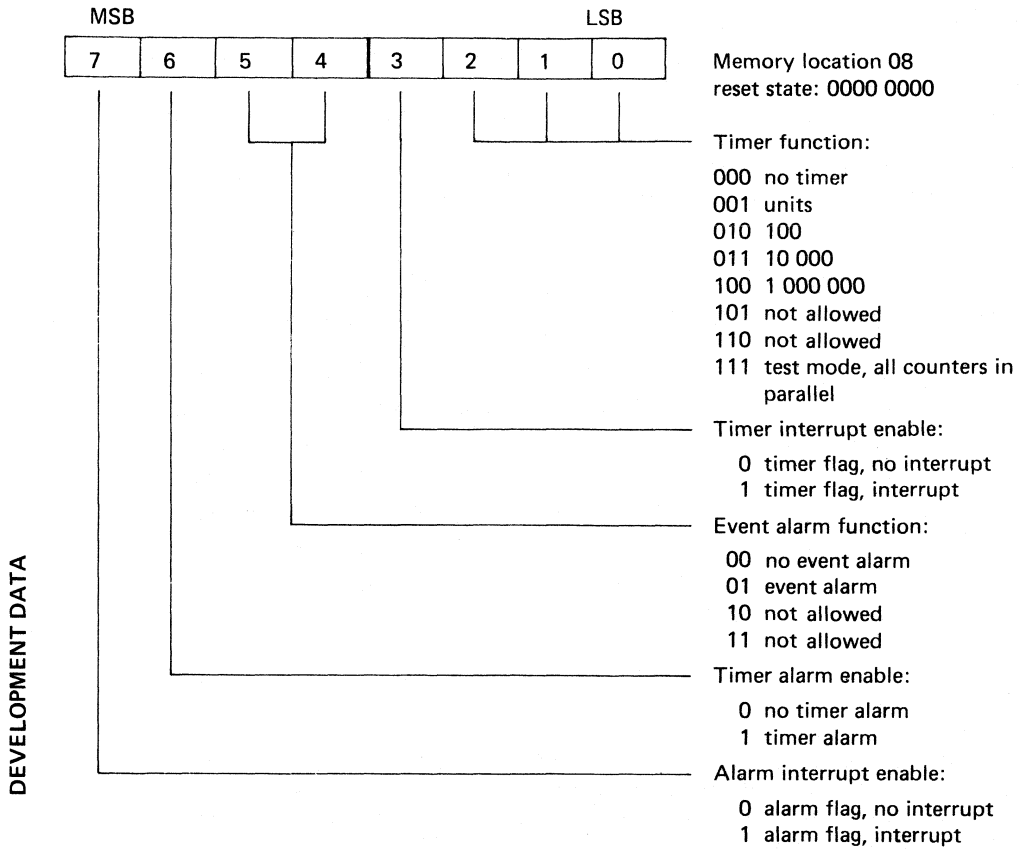


Fig. 8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

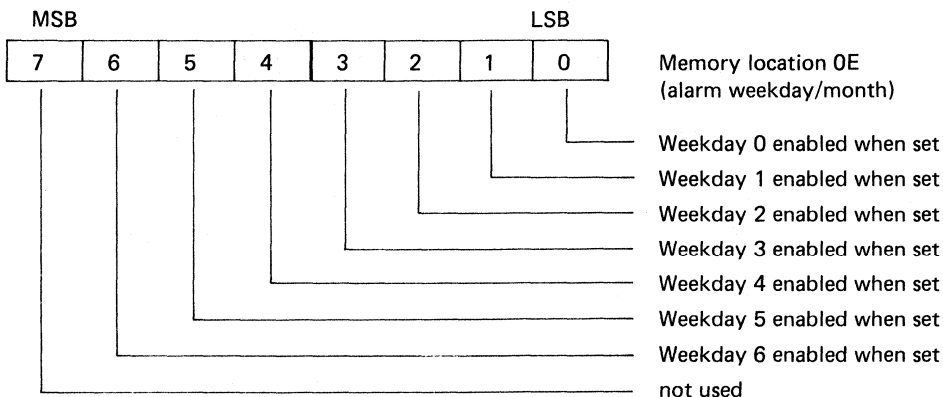


Fig. 9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32,768 kHz quartz crystal has to be connected to OSC1 (pin 1) and OSC0 (pin 2). A trimmer capacitor between OSC1 and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128 Hz by the divider. A 100 Hz clock signal is derived from this signal.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSC1.

Initialization

When power-up occurs the I²C bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32,768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00.

A second level-sensitive reset signal to the I²C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

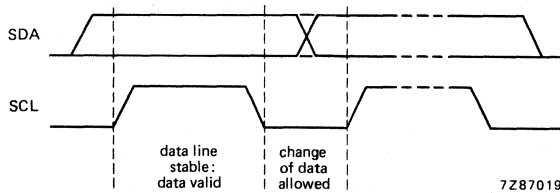


Fig. 10 Bit transfer.

DEVELOPMENT DATA

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

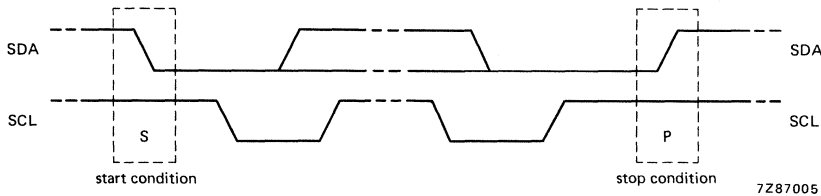


Fig. 11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

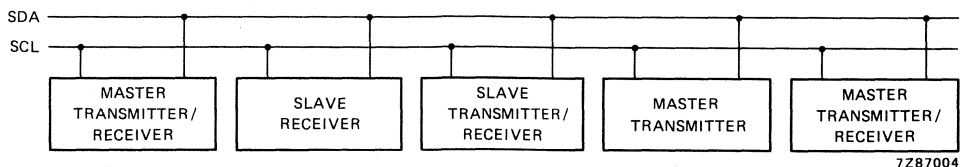


Fig. 12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

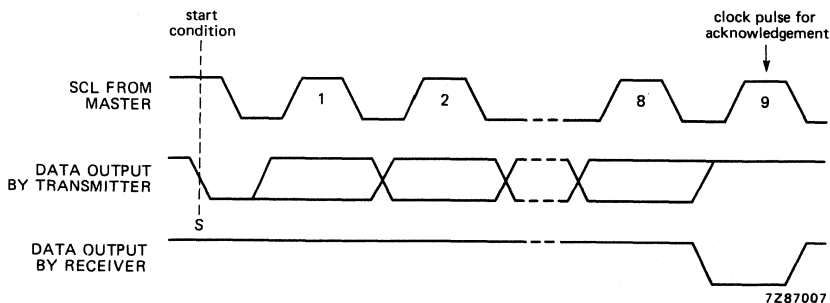


Fig. 13 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} .

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	—	—	100	kHz
Tolerable spike width on bus	t_{SW}	—	—	100	ns
Bus free time	t_{BUF}	4,0	—	—	μ s
Start condition set-up time	$t_{SU}; STA$	4,0	—	—	μ s
Start condition hold time	$t_{HD}; STA$	4,7	—	—	μ s
SCL LOW time	t_{LOW}	4,7	—	—	μ s
SCL HIGH time	t_{HIGH}	4,0	—	—	μ s
SCL and SDA rise time	t_R	—	—	1,0	μ s
SCL and SDA fall time	t_F	—	—	0,3	μ s
Data set-up time	$t_{SU}; DAT$	250	—	—	ns
Data hold time	$t_{HD}; DAT$	0	—	—	ns
SCL LOW to data out valid	$t_{VD}; DAT$	—	—	3,4	μ s
Stop condition set-up time	$t_{SU}; STO$	4,0	—	—	μ s

DEVELOPMENT DATA

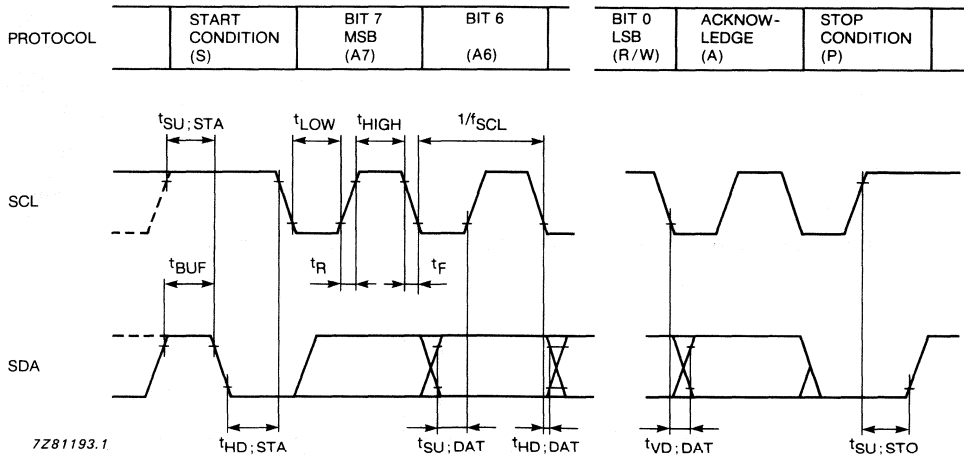


Fig. 14 I²C bus timing diagram.

I²C bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig. 15.

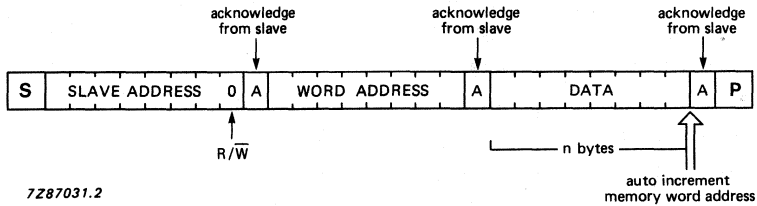


Fig. 15a Master transmits to slave receiver (WRITE mode).

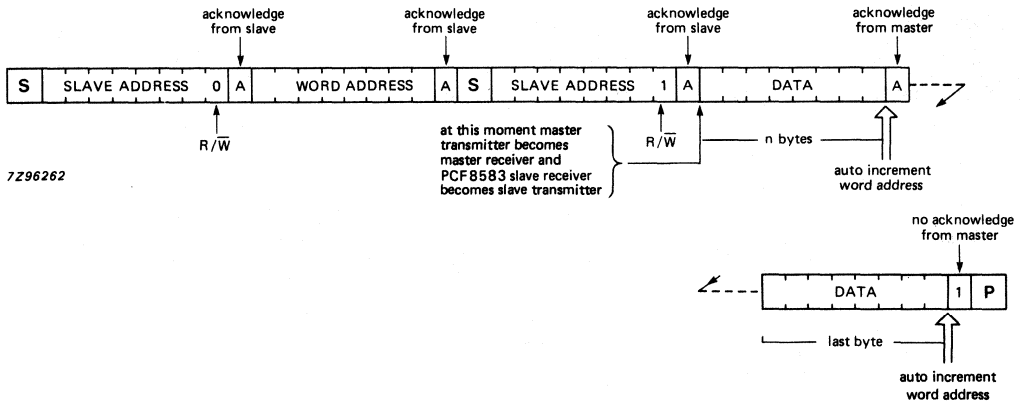


Fig. 15b Master reads after setting word address (WRITE word address; READ data).

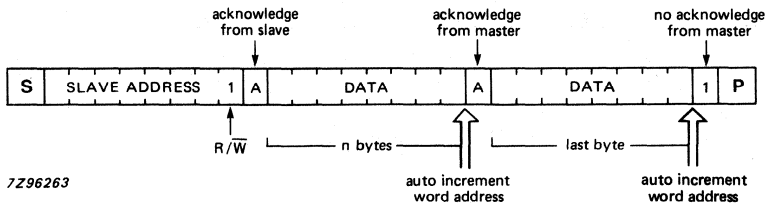


Fig. 15c Master reads slave immediately after first byte (READ mode).

CHARACTERISTICS

$V_{DD} = 2,5$ to $6,0$ V; $V_{SS} = 0$ V; $T_{amb} = -40$ to $+85$ °C unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	—	6	V
Supply current at $V_I = V_{SS}$ or V_{DD} operating at $f_{SCL} = 100$ kHz	I_{DD}	—	—	200	μA
standby at $f_{SCL} = 0$ kHz	I_{DDO}	—	—	15	μA
standby at $T_{amb} = -25$ to $+70$ °C	I_{DDO}	—	—	5	μA
Power-on reset voltage level (note 1)	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW (note 2)	V_{IL}	-0,8	—	$0,3 \times V_{DD}$	V
Input voltage HIGH (note 2)	V_{IH}	$0,7 \times V_{DD}$	—	$V_{DD} + 0,8$	V
Output current LOW at $V_{OL} = 0,4$ V	I_{OL}	3	—	—	V
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	—	—	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	—	—	250	nA
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	—	—	7	pF
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	—	6	V
Supply current at $V_{DDR} = 1$ V	I_{DDR}	—	—	5	μA
Supply current at $V_{DDR} = 1$ V; $T_{amb} = -25$ to $+70$ °C	I_{DDR}	—	—	2	μA
Oscillator					
Integrated oscillator capacitance	C_{OSC}	—	40	—	pF
Oscillator stability for: $\Delta V_{DD} = 100$ mV at $V_{DD} = 1,5$ V; $T_{amb} = 25$ °C	f/f_{OSC}	—	2×10^{-6}	—	—

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	—	—	40	$K\Omega$
Parallel capacitance	C_L	—	9	—	pF
Trimmer capacitance	C_T	5	—	25	pF

Notes to characteristics

1. The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed $\pm 0,5$ mA.

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

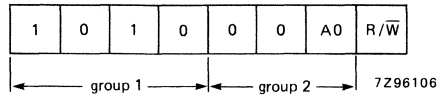


Fig. 16 PCF8583 address.

DEVELOPMENT DATA

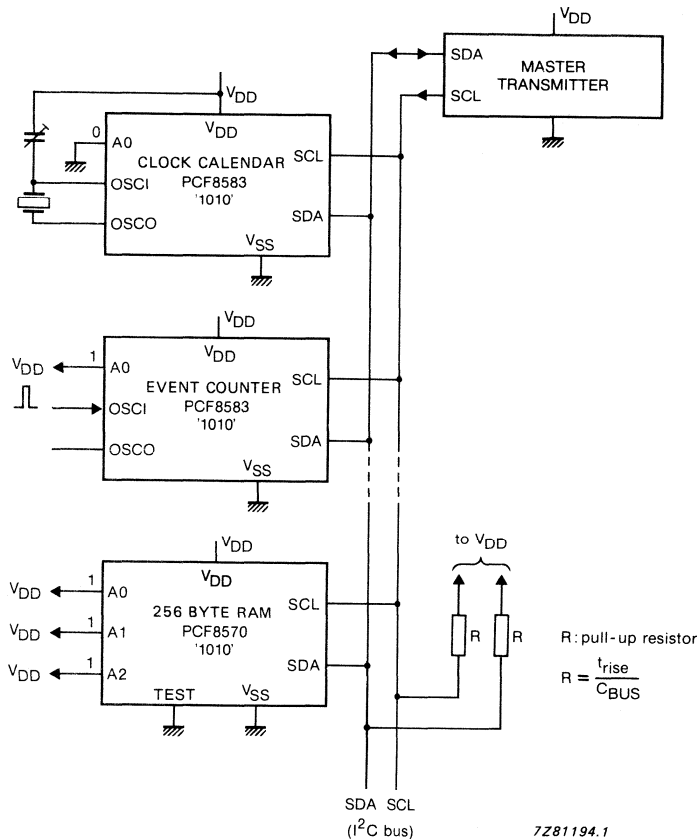
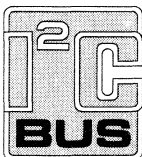


Fig. 17 PCF8583 application diagram.

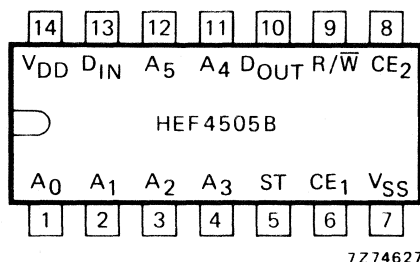


Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

64-BIT, 1-BIT PER WORD RANDOM ACCESS READ/WRITE MEMORY



The HEF4505B is a 64-bit, 1-bit per word, fully decoded and completely static, random access memory. The memory is strobed for reading or writing only when the strobe input (ST), chip enable inputs (CE₁ and CE₂) are HIGH simultaneously. The output data is available at the data output (D_{OUT}) only when the memory is strobed, the read/write input (R/ \bar{W}) is HIGH and after the read access time has passed. Note that the three-state output is initially disabled and always goes to the LOW state before data is valid. The output is disabled in the high-impedance OFF-state, when the memory is not strobed or R/ \bar{W} is LOW. R/ \bar{W} may remain HIGH during a read cycle or LOW during a write cycle. The output data has the same polarity as the input data.



HEF4505BP : 14-lead DIL; plastic (SOT-27 KE, ME, MF). ◀
HEF4505BD : 14-lead DIL; ceramic (SOT-73A, B, C). ▶

Fig. 1 Pinning diagram.

PINNING

A₀ to A₅ address inputs
CE₁, CE₂ chip enable inputs
R/ \bar{W} read/write input
ST strobe input
D_{IN} data input
D_{OUT} data output

FUNCTION TABLE

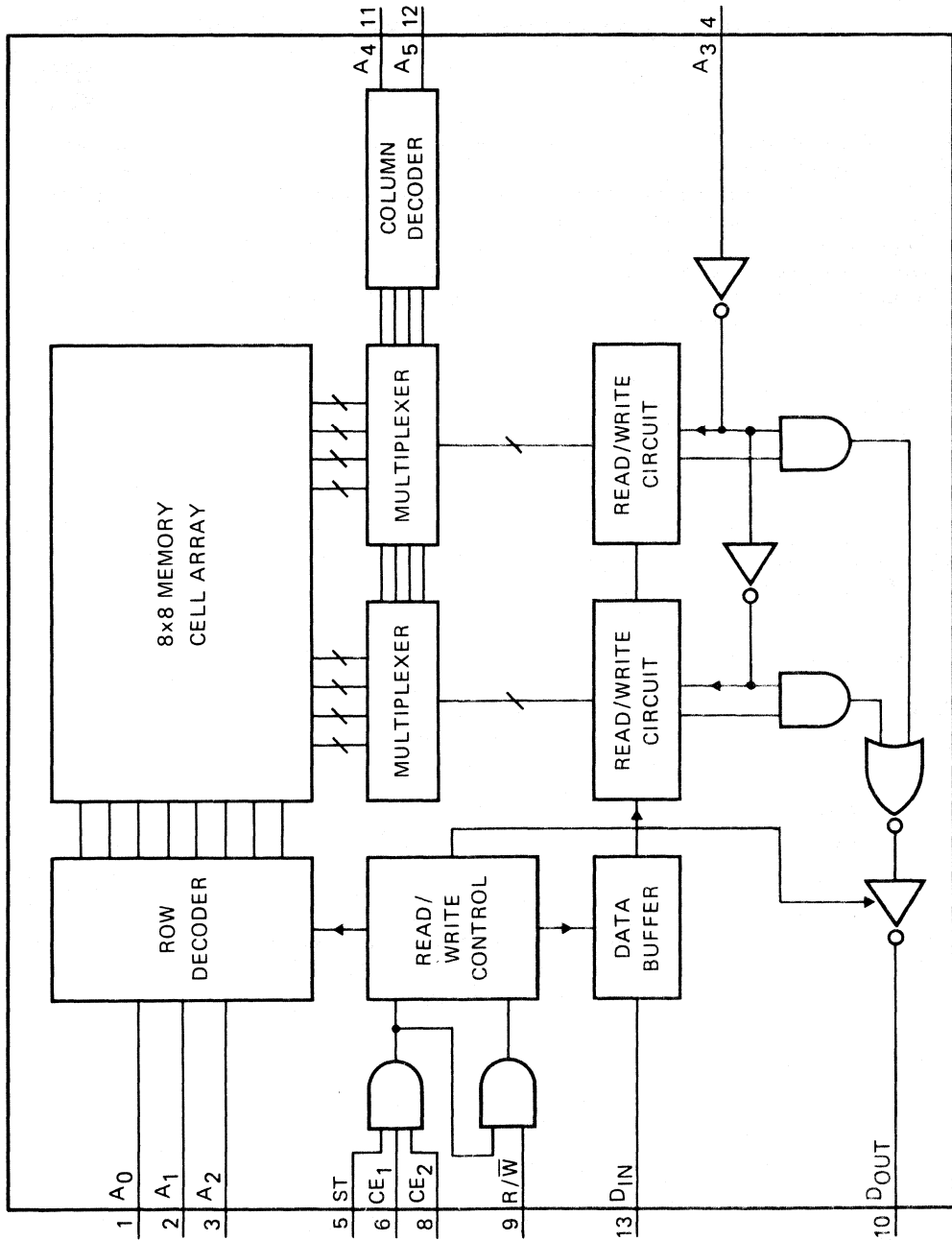
ST, CE ₁ , CE ₂	R/ \bar{W}	D _{OUT}	mode
L	L	Z	disabled
H	L	Z	write
L	H	Z	disabled
H	H	equal to memory data	read

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
Z = high-impedance OFF-state

FAMILY DATA

I_{DD} LIMITS category LSI

} see Family Specifications



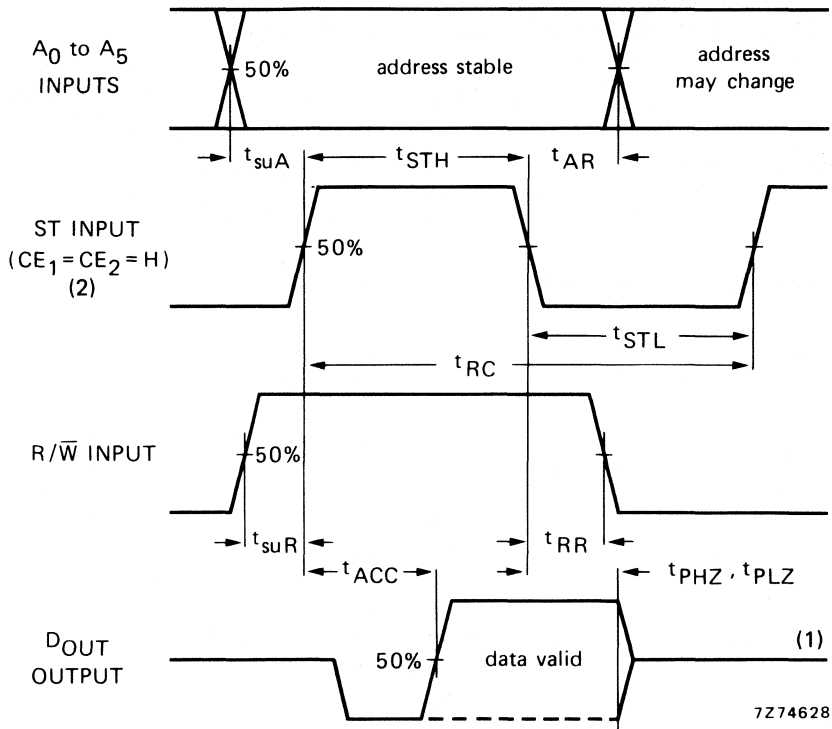
7274630.2

Fig. 2 Functional diagram.

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

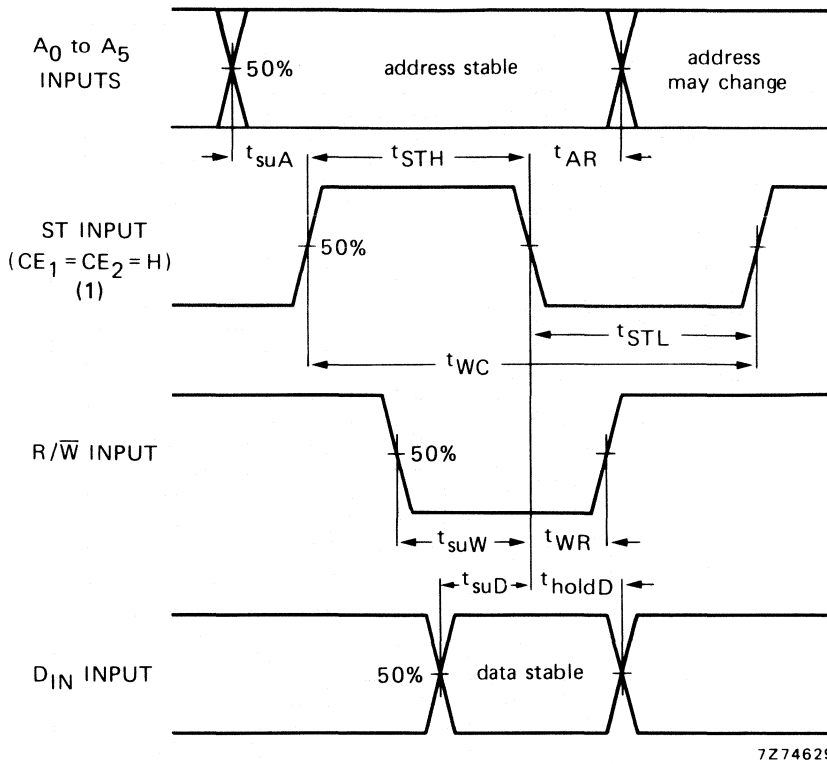
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Minimum strobe pulse width; LOW	5	tSTL	75	35	ns		
	10		45	22	ns		
	15		30	15	ns		
Read cycle time	5	tRC		350	700		ns
	10			250	500		ns
	15			210	420		ns
Write cycle time	5	tWC		220	440		ns
	10			125	250		ns
	15			75	150		ns
Read access time	5	tACC		330	660		ns
	10			135	270		ns
	15			100	200		ns
Address recovery time	5	tAR	80	40	ns		$303\text{ ns} + (0,55\text{ ns/pF}) C_L$ $124\text{ ns} + (0,23\text{ ns/pF}) C_L$ $92\text{ ns} + (0,16\text{ ns/pF}) C_L$
	10		40	20	ns		
	15		25	10	ns		
Read recovery time	5	tRR	180	90	ns		
	10		120	60	ns		
	15		90	45	ns		
Write recovery time	5	tWR	75	35	ns		
	10		45	25	ns		
	15		40	20	ns		
3-state propagation delays							
Output disable times	5	tPHZ, tPLZ		105	210	ns	
	10			60	125	ns	
	15			55	115	ns	
Set-up times $A_n \rightarrow \text{ST}$	5	t _{suA}	-20	-40	ns		
	10		-10	-20	ns		
	15		-5	-10	ns		
$R/\bar{W} \rightarrow \text{ST}$	5	t _{suR}	-30	-60	ns		
	10		-15	-30	ns		
	15		-5	-10	ns		
$D_{IN} \rightarrow \text{ST}$	5	t _{suD}	160	80	ns		
	10		75	35	ns		
	15		45	20	ns		
$R/\bar{W} \rightarrow \text{ST}$	5	t _{suW}	240	120	ns		
	10		100	50	ns		
	15		75	35	ns		
Hold time $D_{IN} \rightarrow \text{ST}$	5	t _{holdD}	-20	-40	ns		
	10		5	-10	ns		
	15		10	0	ns		



(1) Output in high impedance OFF-state.

(2) $t_{STHmin} = t_{RCmax} - t_{STLmin}$.

Fig. 3 Read cycle timing diagram.



(1) $t_{STHmin} = t_{WCmax} - t_{STLmin}$.

Fig. 4 Write cycle timing diagram.

APPLICATION INFORMATION

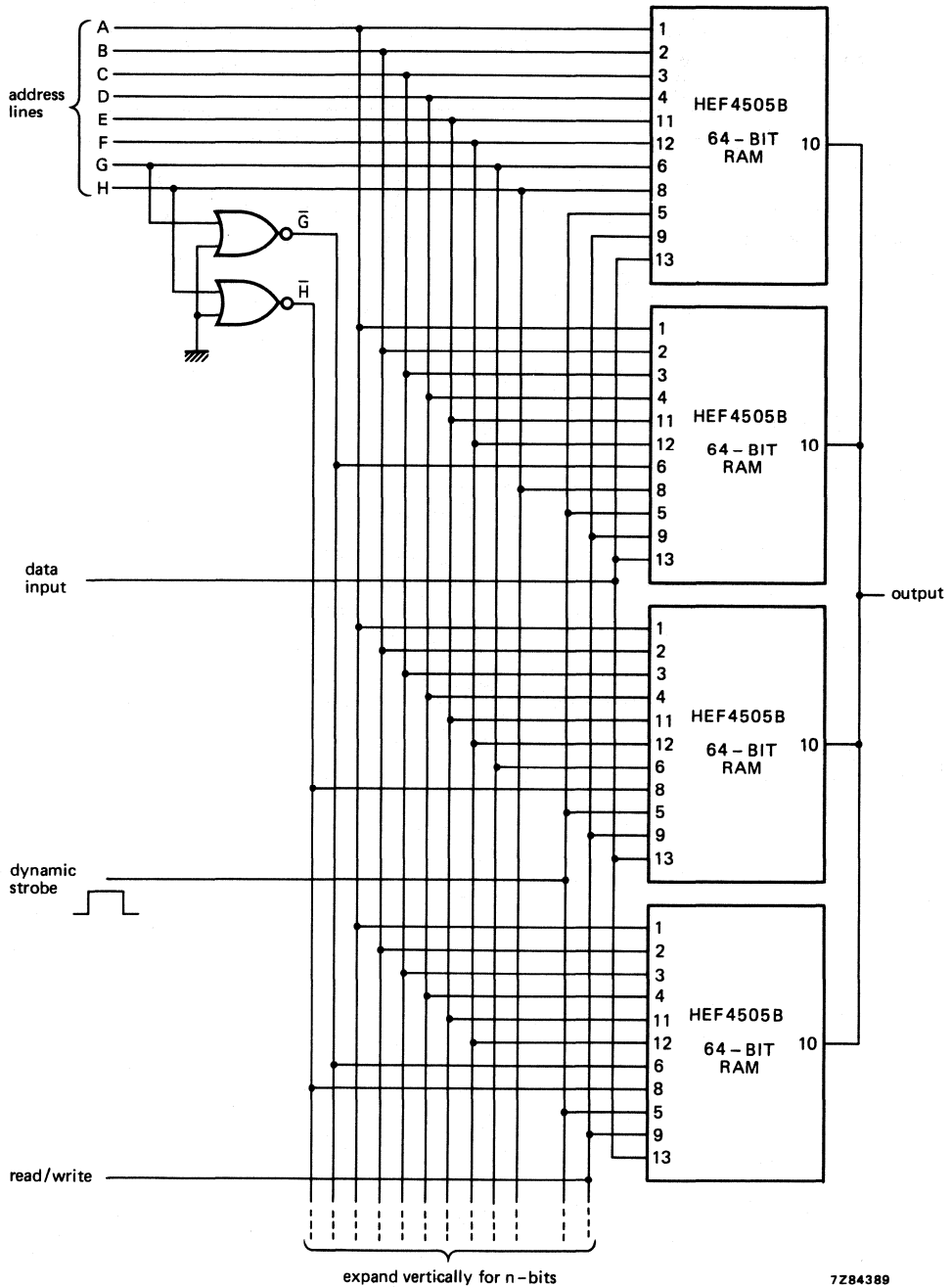


Fig. 5 256-word by n-bit static read/write memory using HEF4505B ICs.

Figure 5 shows a 256-word by n-bit static RAM system. The outputs of the four HEF4505B circuits are tied together to form 256 words by 1-bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and AND-ing them with the strobe input.

Fan-in and fan-out of the memory are limited only by speed requirements. The extremely low input and output leakage currents keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

The memory system shown in Fig. 5 can be interfaced directly with other ICs of the LOCMOS HE family. No external components are required.

Non-volatile information storage is allowed due to very low power dissipation when the memory is powered by a small standby battery. Figure 6 shows an optional standby power supply circuit for making a LOCMOS memory 'non-volatile'. When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor (R) which sets the charging rate. In Fig. 6 the sustaining voltage is V_B , and +V is the ordinary voltage from a power supply. V_{DD} is connected to the power supply pin of the memory. Low-leakage diodes are recommended to conserve battery power.

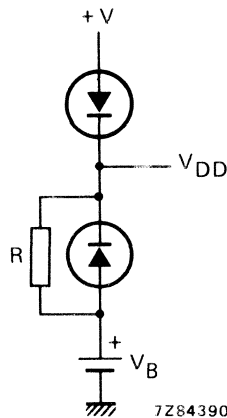


Fig. 6 Standby battery circuit.

256-BIT, 1-BIT PER WORD RANDOM ACCESS MEMORIES

The HEF4720B and HEF4720V are 256-bit, 1-bit per word random access memories with 3-state outputs. The memories are fully decoded and completely static.

Recommended supply voltage range for HEF4720B is 3 to 15 V and for HEF4720V is 4,5 to 12,5 V; minimum stand-by voltage for both types is 3 V.

The use of LOC MOS gives the added advantage of very low stand-by power. The circuits can be directly interfaced with standard bipolar devices (TTL) without using special interface circuits. The memory operates from a single power supply. The separate chip select input (\overline{CS}) allows simple memory expansion when the outputs are wire-ORed. If \overline{CS} is HIGH, the outputs are floating and no new information can be written into the memory. The signal at \overline{O} has the same polarity as the data input D, while the signal at O is the complement of the signal at \overline{O} . The write control W must be HIGH for writing into the memory.

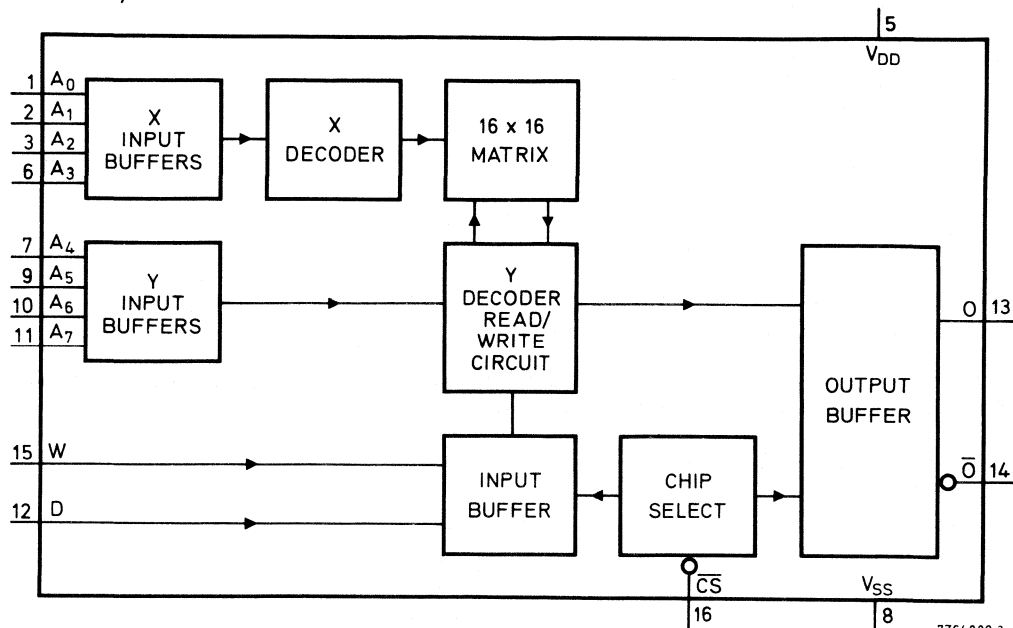


Fig. 1 Functional diagram.

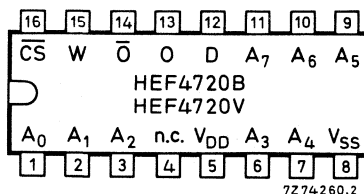


Fig. 2 Pinning diagram.

HEF4720BP; HEF4720VP: 16-lead DIL; plastic (SOT-38 ZE).

HEF4720BD; HEF4720VD: 16-lead DIL; ceramic (cerdip) (SOT-74 A,B,C).

HEF4720BT; HEF4720VT: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

FAMILY DATA: see Family Specifications.

I_{DD} LIMITS: see next page.

FUNCTION TABLE

\overline{CS}	W	O	\overline{O}	mode
L	H	data written into memory	complement of data written into memory	write
L	L	data written into memory	complement of data written into memory	read
H	X	Z	Z	inhibit

H = HIGH state (the more positive voltage) X = state is immaterial
L = LOW state (the less positive voltage) Z = high impedance OFF-state

PINNING

- \overline{CS} chip select input (active LOW)
- W write enable input
- D data input
- A₀ to A₇ address inputs
- O 3-state output (active HIGH)
- \overline{O} 3-state output (active LOW)

SUPPLY VOLTAGE

	rating	recommended operating	stand-by min.
HEF4720B	-0,5 to 18	3,0 to 15,0	3 V
HEF4720V	-0,5 to 18	4,5 to 12,5	3 V

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4720V, because of its lower supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V _{DD} V	V _{OL} V	symbol	T _{amb} (°C)					
				-40		+25		+85	
				min.	max.	min.	max.	min.	max.
Output current LOW	4,75	0,4	I _{OL}	2,4	2	1,6			
	10	0,5		4,8	4	3,2			
	15	1,5		10,0	10	7,5			
Quiescent device current	5		I _{DD}		25	25		200	
	10				50	50		400	
	15				100	100		800	
Input leakage current	10		±I _{IN}		0,3	0,3		1	
	15				0,3	0,3		1	

A.C. CHARACTERISTICS

	V _{DD} V	symbol	min.	typ.	max.	
Output capacitance	5	C _O		5		pF
	10			5		pF
	15			5		pF

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Read cycle							
Read access time	5	t _{ACC}		320	580	ns	292 ns + (0,55 ns/pF) C _L
	10			130	220	ns	118 ns + (0,23 ns/pF) C _L
	15			100	160	ns	92 ns + (0,16 ns/pF) C _L
Chip select to output time	5	t _{CO}			180	ns	
	10				70	ns	
	15				50	ns	
Address hold time	5	t _{OA}	0			ns	
	10		0			ns	
	15		0			ns	
Output hold time with respect to address input	5	t _{VAL1}	60	170		ns	142 ns + (0,55 ns/pF) C _L
	10		20	50		ns	38 ns + (0,23 ns/pF) C _L
	15		15	40		ns	32 ns + (0,16 ns/pF) C _L
Output hold time with respect to chip select input	5	t _{COH}			130	ns	
	10				70	ns	
	15				60	ns	
Output floating time with respect to chip select input	5	t _{COF}	0			ns	
	10		0			ns	
	15		0			ns	
Read cycle time	5	t _{RC}	580			ns	
	10		220			ns	
	15		160			ns	
Output transition times LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L
HIGH to LOW	5	t _{THL}		40	80	ns	14 ns + (0,52 ns/pF) C _L
	10			22	40	ns	11 ns + (0,22 ns/pF) C _L
	15			15	30	ns	7 ns + (0,16 ns/pF) C _L

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.
Write cycle					
Write cycle time	5	t_{WC}	580		ns
	10		220		ns
	15		160		ns
Address to write set-up time	5	t_{AW}	110		ns
	10		50		ns
	15		50		ns
Write pulse width	5	t_{WP}	370	10 000	ns
	10		130	10 000	ns
	15		80	10 000	ns
Write recovery time	5	t_{WR}	100		ns
	10		40		ns
	15		30		ns
Data set-up time	5	t_{DW}	250		ns
	10		100		ns
	15		80		ns
Data hold time	5	t_{DH}	100		ns
	10		30		ns
	15		20		ns
Chip select set-up time with respect to write pulse	5	t_{CSW}	370		ns
	10		130		ns
	15		80		ns
Chip select hold time with respect to write pulse	5	t_{CSH}	0		ns
	10		0		ns
	15		0		ns
Chip select lead time over write pulse to prevent writing	5	t_{CSL}	0		ns
	10		0		ns
	15		0		ns
Read-modify-write cycle					
Read enable hold time	5	t_{RH}	0		ns
	10		0		ns
	15		0		ns
Output hold time with respect to write pulse	5	t_{VAL2}	60		ns
	10		20		ns
	15		15		ns
Read-modify-write cycle time	5	t_{RWC}	1050		ns
	10		390		ns
	15		270		ns

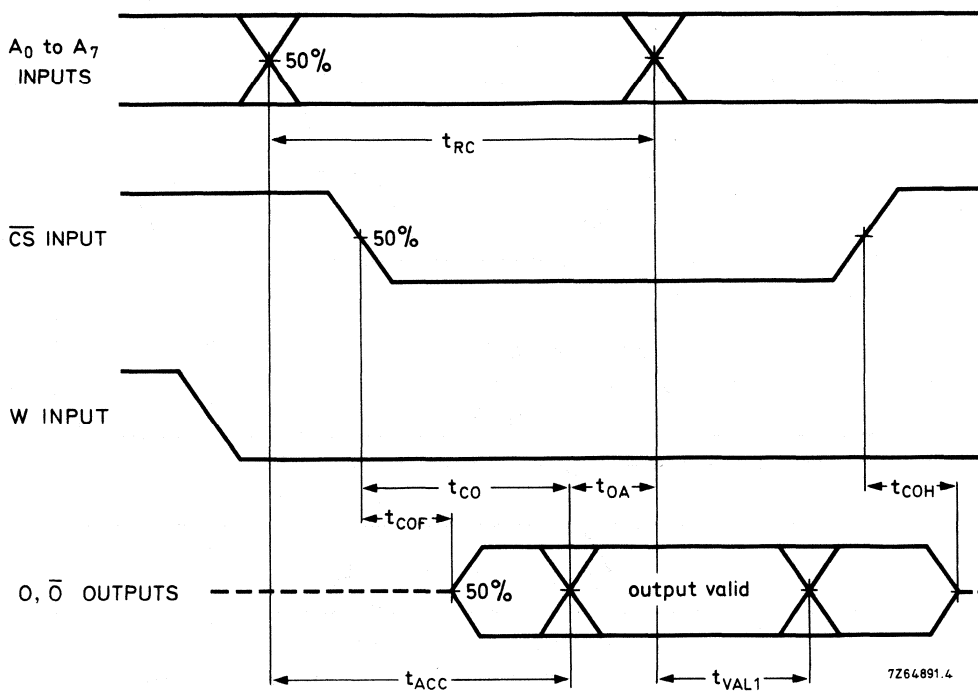


Fig. 3 Read cycle timing diagram.

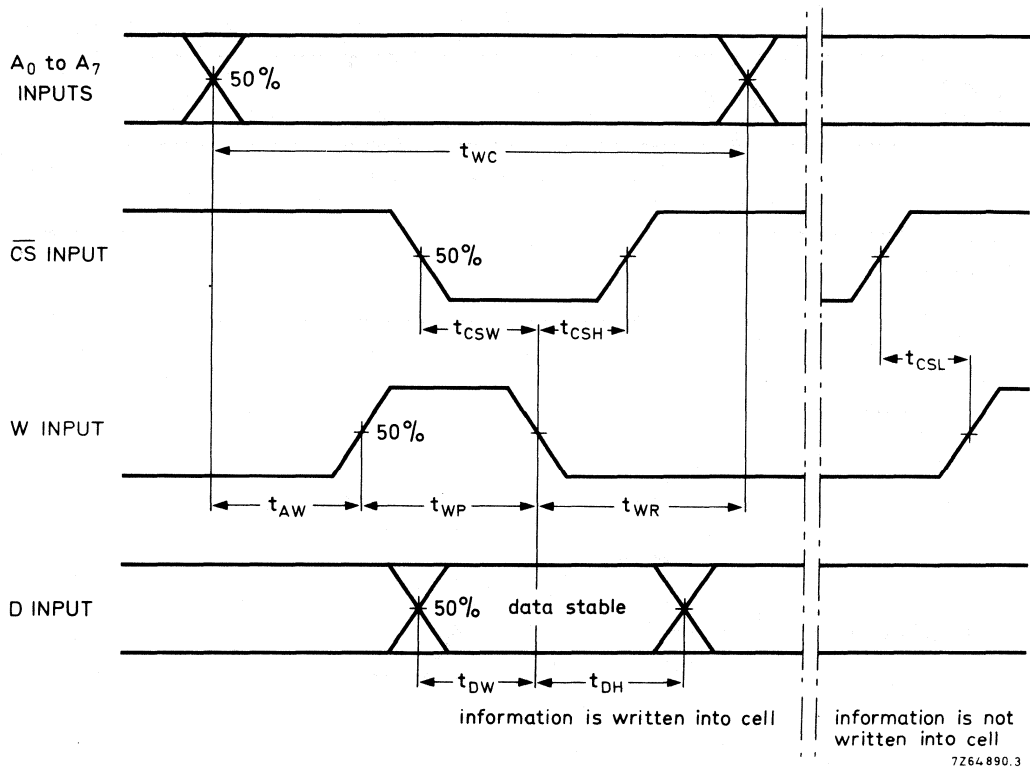
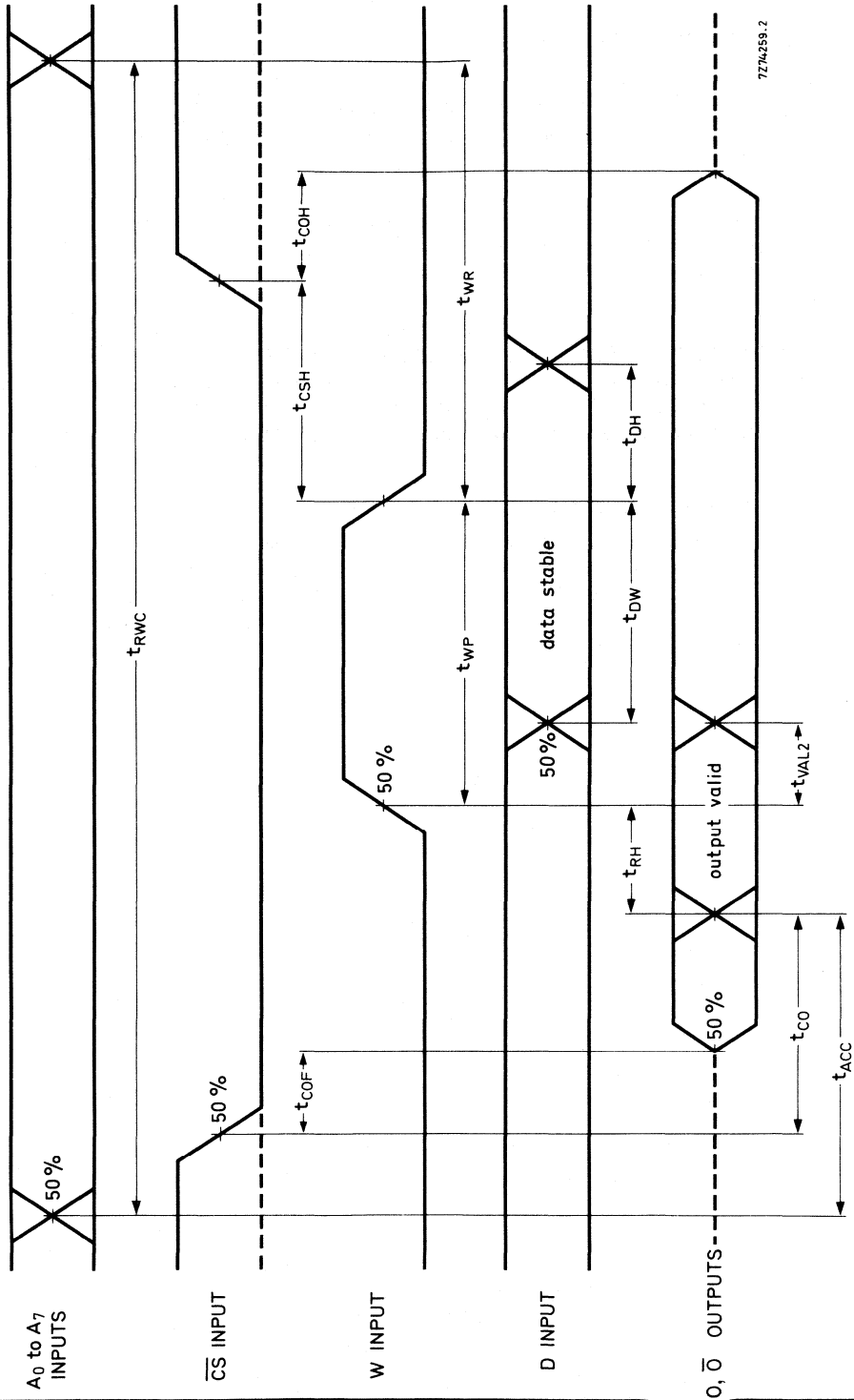


Fig. 4 Write cycle timing diagram.



7274259.2

Fig. 5 Read-modify-write cycle timing diagram.

APPLICATION INFORMATION

Extension of memory capacity

The memory capacity of the HEF4720B; V is 256 bits (or 256 words of 1 bit). The capacity of a system can be extended in various ways by the connection of further HEF4720B; V ICs.

Extending the word length

By connecting a number of HEF4720B; V ICs as shown in Fig. 6, the word length (i.e. bits per word) is multiplied by that number. That is, each device stores 1 bit per word but the total number of words remains 256. For example, if four devices are used in this way, 256 four-binary-bit words can be stored.

Extending the number of words

If a number of HEF4720B; V ICs are connected as shown in Fig. 7, the words available are multiplied by that number, but the word length remains 1 bit. Notice that in this case additional addresses are used in conjunction with the \overline{CS} input. In the case shown in Fig. 7 (4 x HEF4720B; V in parallel), the addresses and data inputs are loaded with four inputs (= 20 pF), the \overline{CS} inputs are loaded with one input each.

Extending both the word length and number of words

Figure 8 shows how a combination of the extensions described above can be used to obtain both greater word length and additional words. It is clear that the capacitive load of the driving circuits puts a limit to the free choice of the interface. In Fig. 8, each address is loaded with 16 inputs, i.e. $16 \times 5 = 80$ pF: each \overline{CS} inverter is loaded with 8 inputs, i.e. $8 \times 5 = 40$ pF. The data inverters in this case are loaded with only two inputs each.

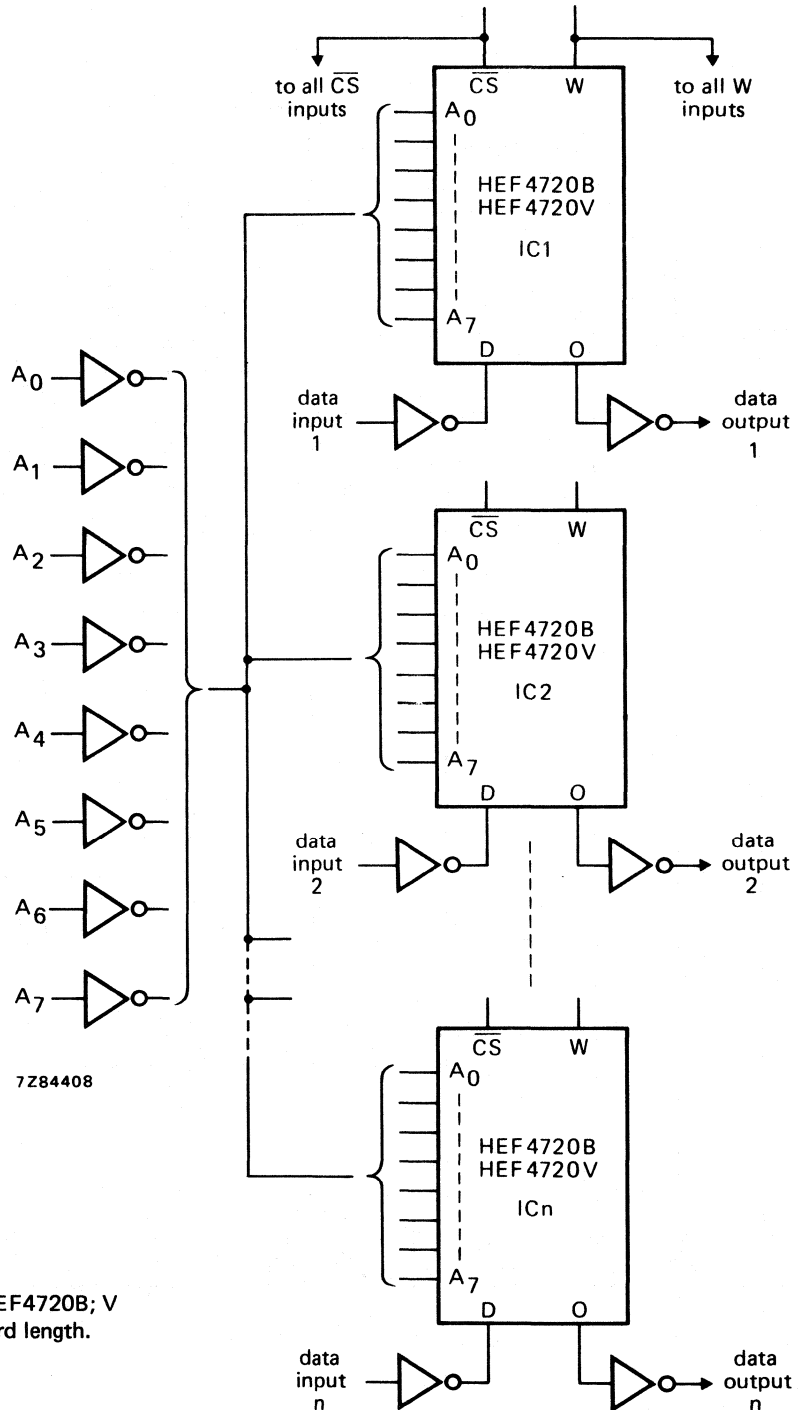


Fig. 6 Using extra HEF4720B; V ICs to extend the word length.

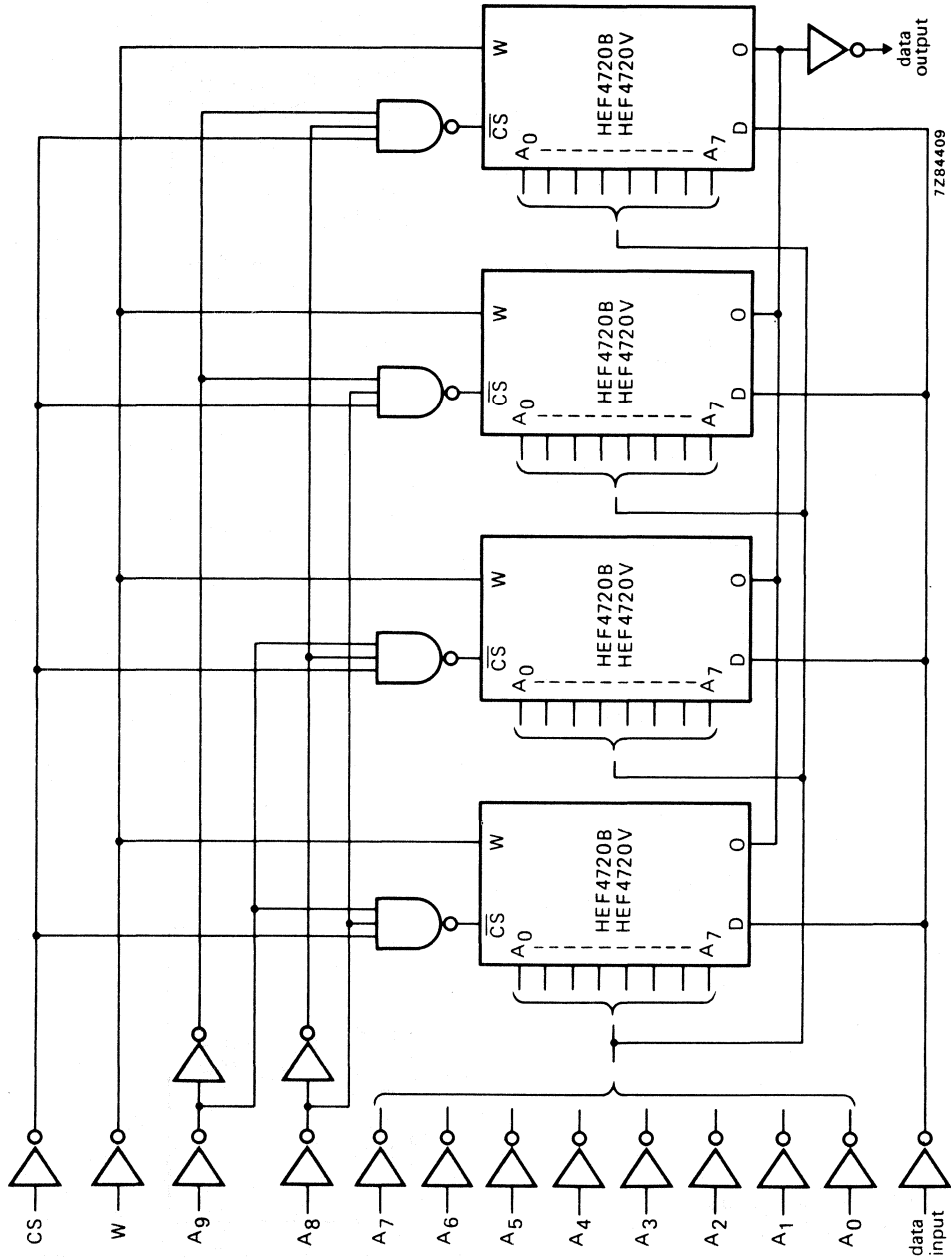
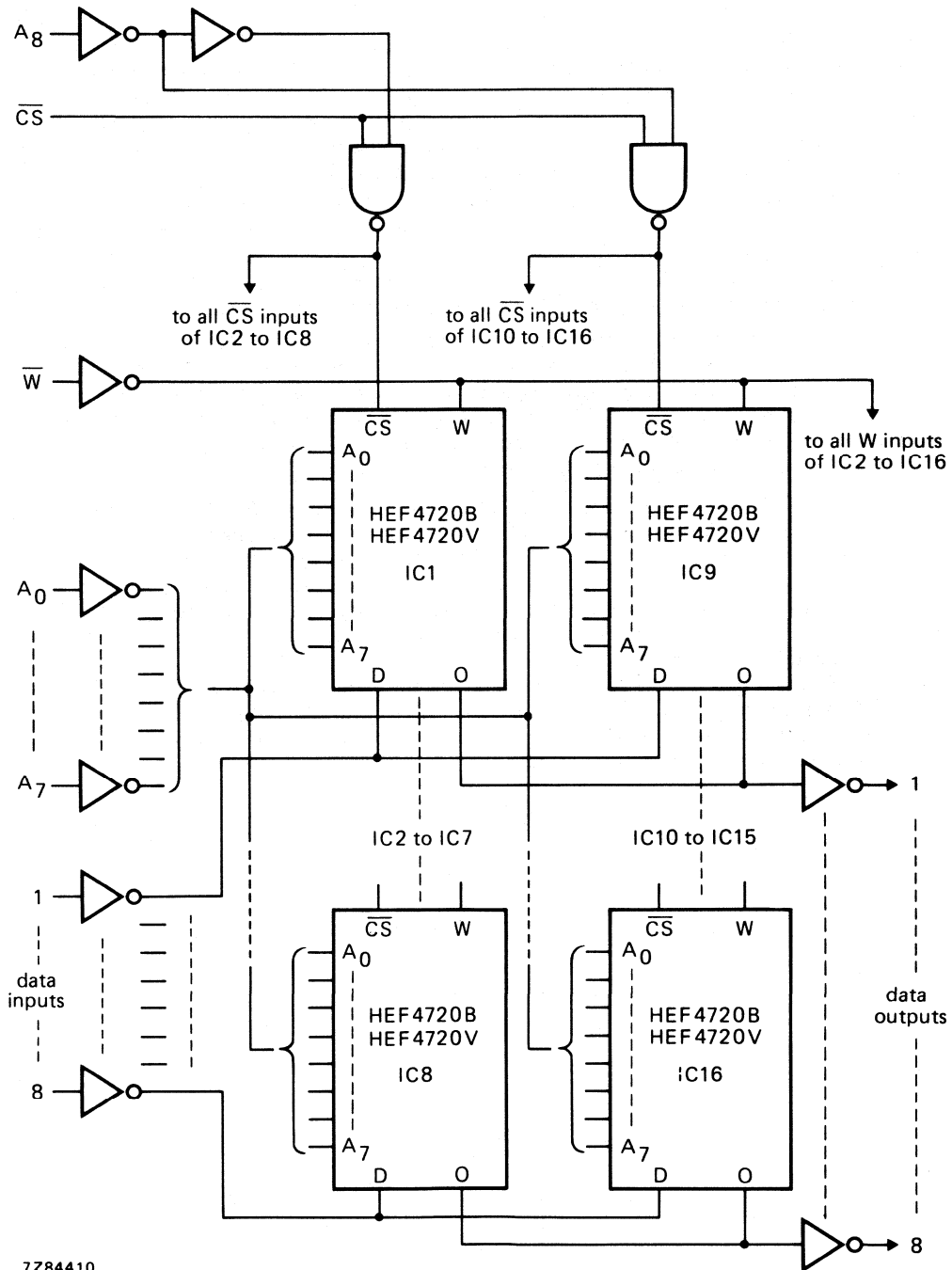


Fig. 7 Using extra HEF4720B; V ICs to obtain more words.



7284410

Fig. 8 Using extra HEF4720B; V ICs to obtain more words and greater word length.

APPLICATION INFORMATION (continued)

Memory retention

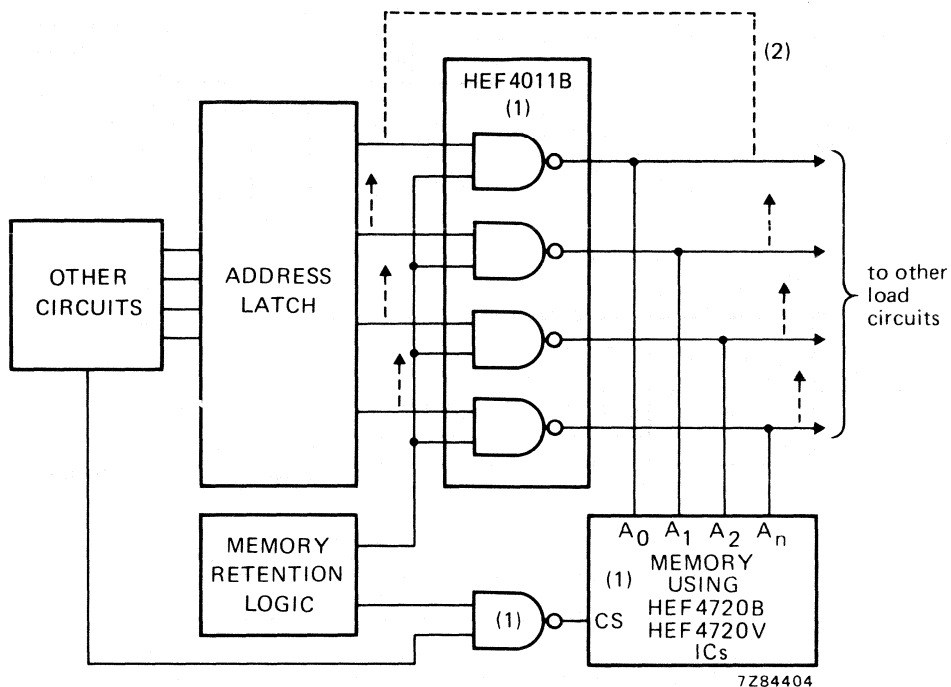
It is sometimes necessary to ensure that the information stored in the memory cannot be erased inadvertently. This can be arranged by adding detection circuits, by measures in the timing, and by the addition of a battery. With the HEF4720B; V, memory retention is very easily obtained because its current drain in the stand-by condition is almost zero. The wide supply voltage range makes it possible to keep the memory active by means of a simple battery, thereby preventing information loss.

In designing the memory retention circuits, two aspects should be kept in mind. The memory retention will not function in an optimum way if the battery voltage is low or if the voltage transitions at the address input are too slow. The first of these is usually the result of using too simple a battery back-up circuit, e.g. a battery charged via a diode from the TTL supply voltage. In this case, the LOCMOS supply voltage falls below the safe operating voltage. Special arrangements should be made to overcome this.

Slow address transitions (the second cause of memory loss) are due to a long RC-time in the power system. When the power is switched on or off, the 5 V line changes between 0 and 5 V in milliseconds to seconds so producing a correspondingly long transition time in the various logic outputs. This creates problems in the proper operation of the HEF4720B; V, with loss of memory as a possible result. This can be prevented by ensuring that input rise and fall times do not exceed 10 μ s.

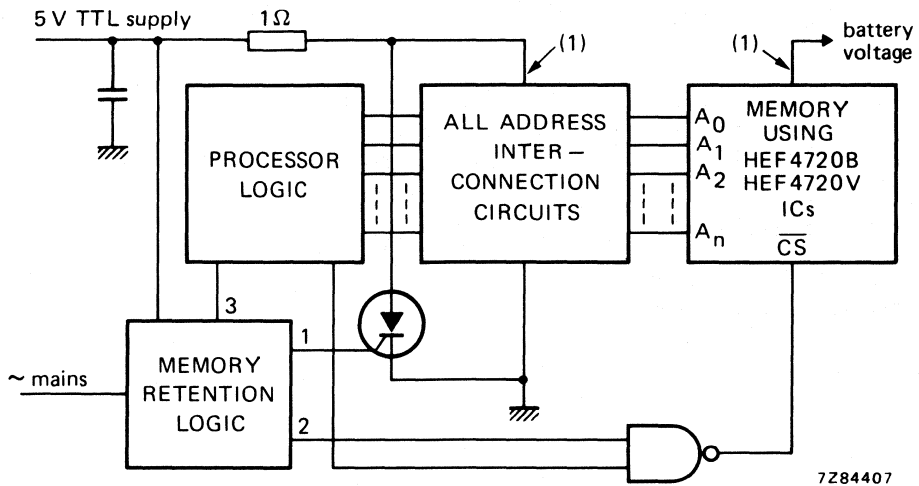
Three possibilities for controlling the rise and fall times at the HEF4720B; V interface are given here:

1. LOCMOS gates can be connected between the address latch and the HEF4720B; V (Fig. 9).
In the event of a low voltage, or mains supply failure, the gates can be blocked by a signal from the memory retention logic thus isolating the HEF4720B; V from the address and \overline{CS} inputs.
2. The interface power supply can be separated from the TTL power supply by means of a low-value resistor (Fig. 10); a thyristor is connected from the interface power supply to earth. The system is arranged so that, upon switching off or failure of the interface supply, the thyristor turns on thus ensuring a rapid fall of the supply voltage.
3. The best solution is to select the interface circuits from the LOCMOS family and to feed all these circuits from the battery (Fig. 11). These stages then remain active when the TTL 5 V supply fails. The interface circuits are mostly only active on a clock pulse, have the possibility of being inactive on a gate level, or can be forced into one position.

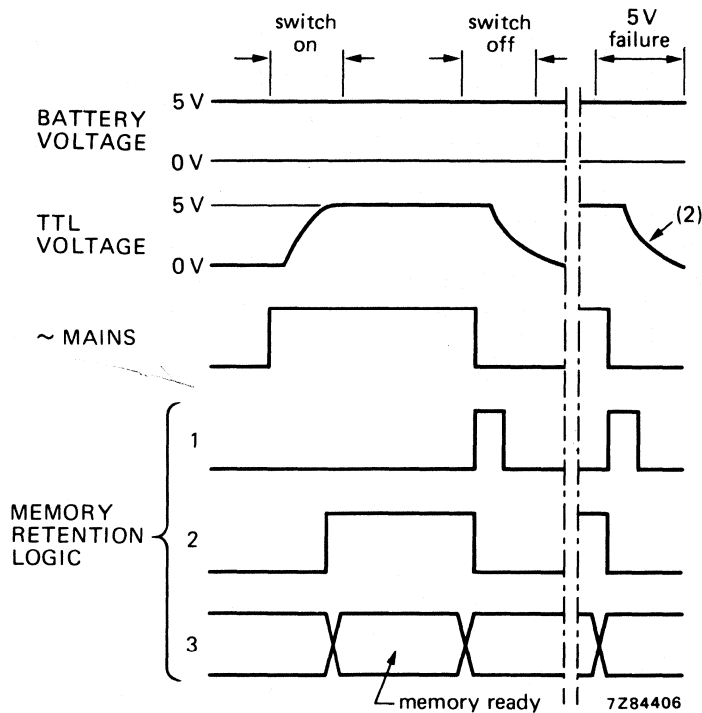


- (1) These devices have a battery supply.
- (2) Alternative connection.

Fig. 9 Use of battery-operated LOCMOS gates to isolate the memory in case of power supply failure. Devices marked (1) are connected to the battery. The HEF4011B can sink about 0,7 mA: if the load is greater than this, only the memory should be connected, other loads being connected to the address latch as shown by the dashed-line connections.



7284407



7284406

- (1) Leads should be so arranged to prevent cross-talk; thyristor connections must be short.
(2) Slope $> 500 \text{ mV}/\mu\text{s}$ in the vicinity of the threshold.

Fig. 10 Using a thyristor to ensure a rapid fall of interface supply at switch-off or supply failure.

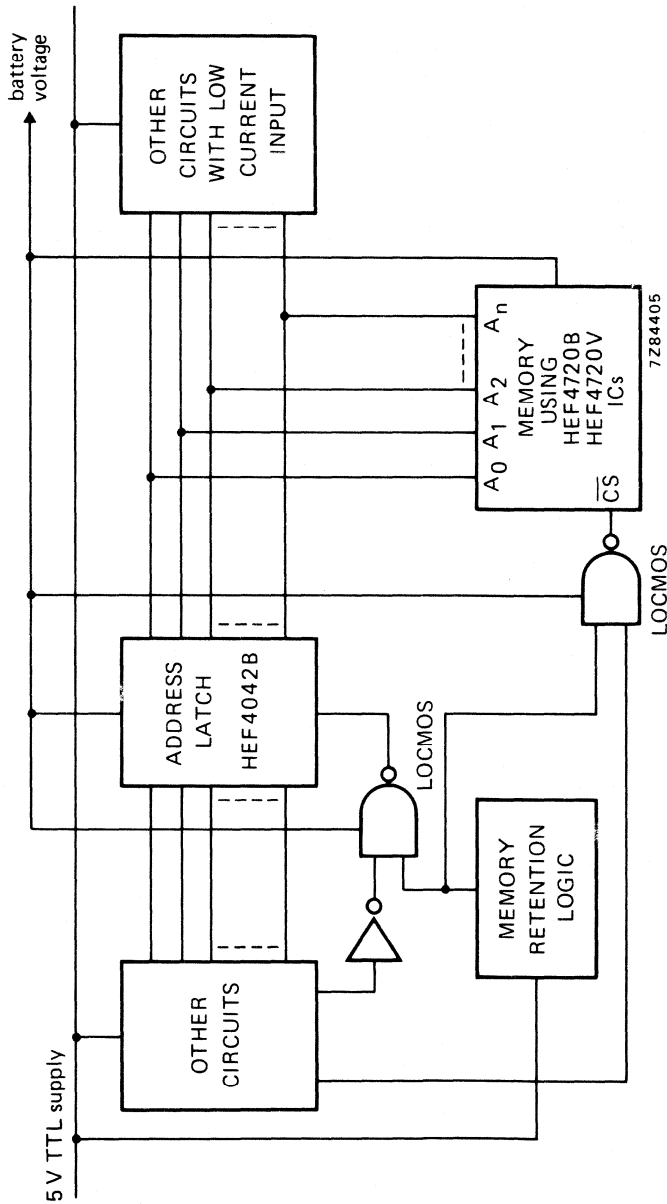


Fig. 11 Preferred solution for memory retention; all interface circuits are battery-fed LOC MOS. Note that maximum sink current of the HEF4042B is about 1,5 mA.

2048 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The SBB6116L is a 16 384-bit static random access memory organized as 2048 words of 8 bits each. A common 8-bit input/output interface is controlled by the output enable (\overline{OE}). A low power/standby mode, controlled by the chip select input (\overline{CS}), is available for memory expansion. The device operates from a 5 V power supply and is available in versions with differing access times (see below). Pin compatibility with EPROM type 2716 allows a wide range of applications in microprocessor peripheral memory design.

Fabrication of this MOS device is by ion implanted complementary silicon gate technology and a process which creates high-ohmic resistors in the memory cell array (CMOS double-poly process).

Features

- Pin-compatible with EPROM type 2716
- Operating supply voltage 5 V
- Choice of access times
- Inputs protected against static charge
- Static operation requiring no clock or timing strobe
- Low power CMOS: 30 μ W (typ.) standby power; 100 mW (typ.) active power
- Address activated: power consumption depends on amount of access
- Easy memory expansion
- Common data input/output interface
- All inputs and outputs directly TTL compatible
- Three-state outputs with wired-OR capability
- Output buffer control
- Suitable for operation with battery back-up

Maximum access times per version

SBB6116L-10: 100 ns

SBB6116L-12: 120 ns

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

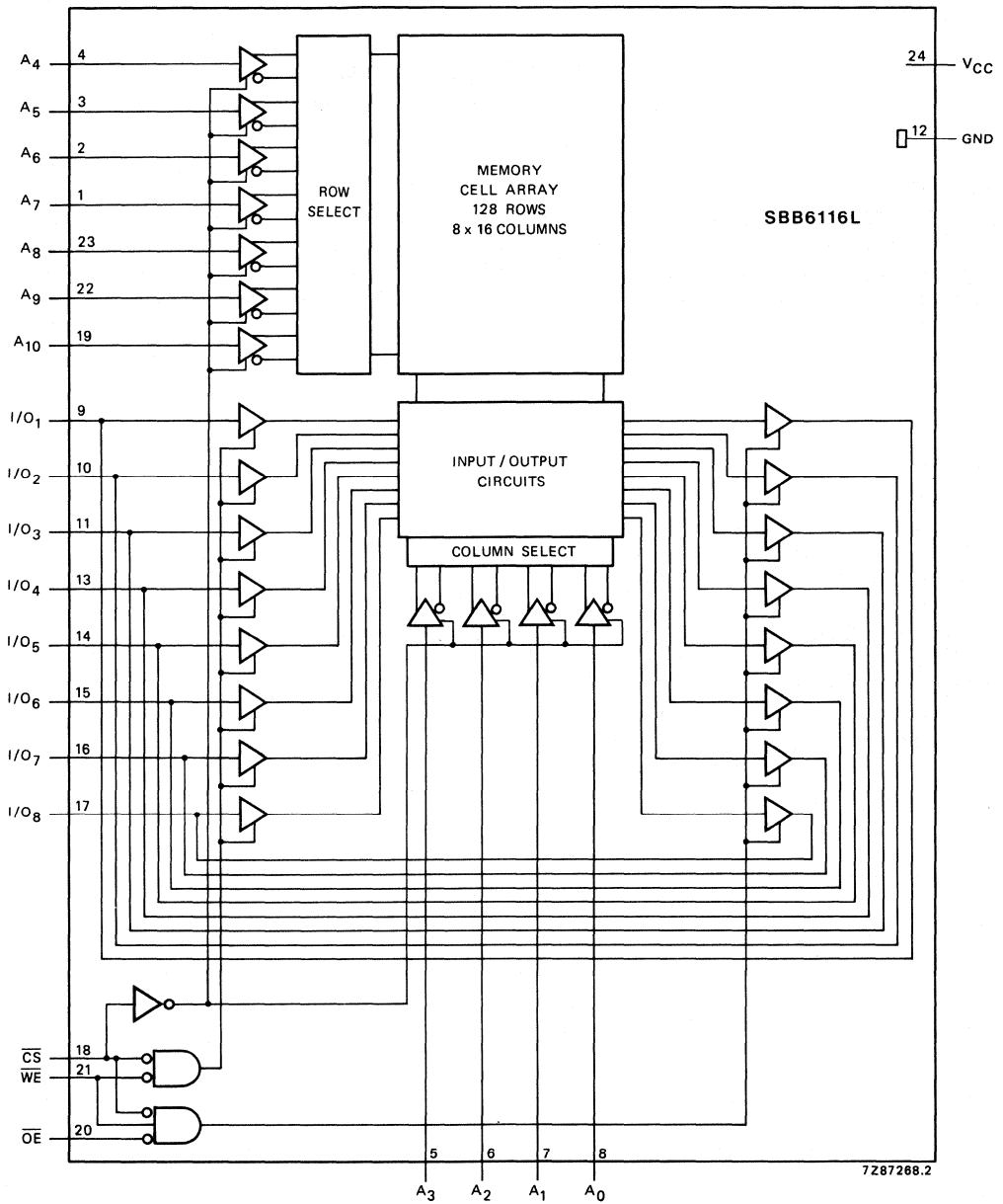
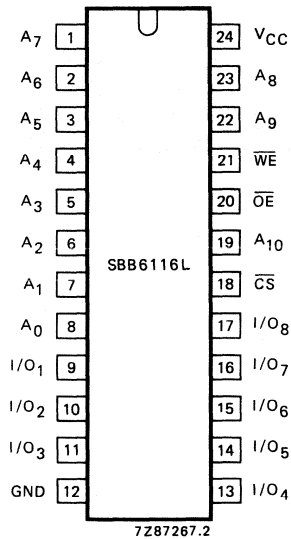


Fig. 1 Block diagram.



PINNING

- A₀ to A₁₀ address inputs
- \overline{CS} chip select input
- \overline{WE} write enable input
- I/O₁ to I/O₈ data input/output
- \overline{OE} output enable input
- V_{CC} positive supply (+ 5 V)
- GND negative supply (ground)

Fig. 2 Pinning diagram.

DEVELOPMENT DATA

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	mode	V _{CC} current	I/O pin	R/W cycle
H	X	X	not selected	I _{SB} , I _{SB1}	Z	
L	L	H	read	I _{CC}	D _O	read cycles 1 to 3
L	H	L	write	I _{CC}	D _I	write cycle 1
L	L	L	write	I _{CC}	D _I	write cycle 2
L	H	H	ready to read; output disbaled	I _{CC}	Z	

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- Z = high impedance OFF-state

DECOUPLING REQUIREMENTS

The SBB6116L static RAM is an address-activated circuit. When an address change occurs, the precharge operation is executed by an internal pulse generated from the address transient. The consequent peak current flow following an address or \overline{CS} change can induce noise on the V_{CC}/GND lines (see Fig. 3). This noise should be eliminated by the use of a 0,1 μF capacitor with good high-frequency characteristic to decouple each device.

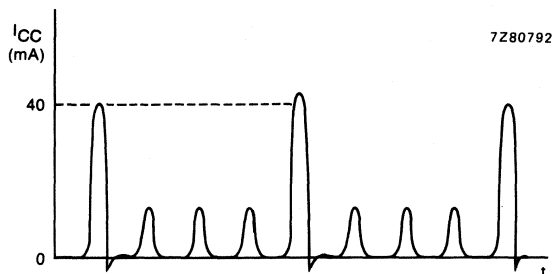


Fig. 3 Typical I_{CC} waveform with address change.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage range on any pin with respect to GND	V_I	-1,0 to +7,0 V
Operating ambient temperature range	T_{amb}	0 to +70 °C
Operating temperature range with bias	T_{bias}	-10 to +85 °C
Storage temperature range	T_{stg}	-55 to +125 °C
Total power dissipation	P_{tot}	1,0 W

RECOMMENDED D.C. OPERATING CONDITIONS

$T_{amb} = 0$ to $+70$ °C; voltages are referenced to GND (0 V)

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	4,5	5,0	5,5	V
Input voltage HIGH	V_{IH}	2,0	3,5	6,0	V
Input voltage LOW	V_{IL}	-0,5*	—	0,8	V

D.C. CHARACTERISTICS

$V_{CC} = 5$ V \pm 10%; $T_{amb} = 0$ to $+70$ °C; voltages are referenced to GND (0 V); unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.**	max.	unit
Input leakage current at $V_{CC} = 5,5$ V; $V_I = \text{GND to } V_{CC}$	$ I_{LI} $	—	—	2,0	μA
Output leakage current at \overline{CS} or $\overline{OE} = V_{IH}$; $V_{I/O} = \text{GND to } V_{CC}$	$ I_{LO} $	—	—	2,0	μA
Operating power supply current at $\overline{CS} = V_{IL}$; $I_{I/O} = 0$ mA (d.c.)	I_{CC}	—	2,0	5,0	mA
Average operating current; minimum cycle time; duty factor 100%; $I_{I/O} = 0$ mA	I_{CC2}	—	20	50	mA
Standby power supply current at $\overline{CS} = V_{IH}$	I_{SB}	—	—	2,0	mA
at $\overline{CS} \geq V_{CC} - 0,2$ V or $\overline{CS} \leq 0,2$ V and $V_I \geq V_{CC} - 0,2$ V or $V_I \leq 0,2$ V	I_{SB1}	—	6,0	100	μA
Output voltage LOW at $I_{OL} = 4$ mA	V_{OL}	—	—	0,4	V
Output voltage HIGH at $I_{OH} = -1,0$ mA	V_{OH}	2,4	—	—	V

CAPACITANCE

$f = 1$ MHz; $T_{amb} = 25$ °C

parameter	symbol	typ.	max.	unit
Input capacitance at $V_I = 0$ V	C_I	3	6	pF
Input/output capacitance at $V_{I/O} = 0$ V	$C_{I/O}$	5	8	pF

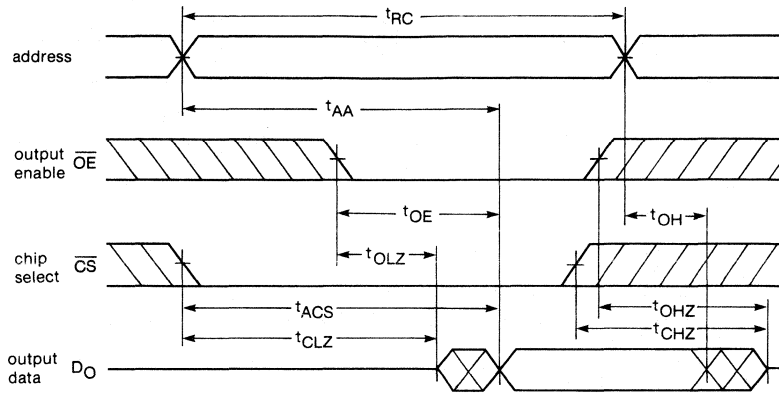
* $V_{IL} = -1$ V with a maximum pulse duration of 50 ns.

** At $V_{CC} = 5$ V; $T_{amb} = 25$ °C.

A.C. CHARACTERISTICS (Figs 4 and 5)

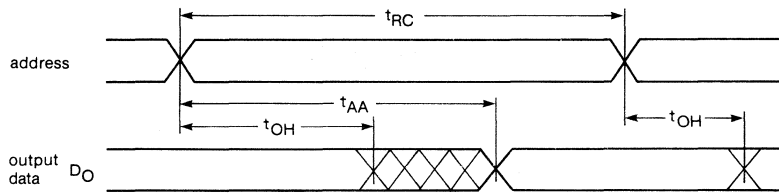
$V_{CC} = 5\text{ V} \pm 10\%$; $T_{amb} = 0\text{ to }+70\text{ }^{\circ}\text{C}$; input pulse levels = 0,4 to 2,4 V; input rise and fall times = 5 ns; input timing reference levels = 1,5 V; output timing reference levels = 0,6 and 2,2 V; output load = 1 TTL gate and capacitance (C_L) = 100 pF (including oscilloscope and jig).

parameter	symbol	6116-10		6116-12		unit
		min.	max.	min.	max.	
Read cycle						
Read cycle time	t_{RC}	100	—	120	—	ns
Address access time	t_{AA}	—	100	—	120	ns
Chip select access time	t_{ACS}	—	100	—	120	ns
Chip select to output in low impedance state	t_{CLZ}	10	—	10	—	ns
Output enable to output valid	t_{OE}	—	50	—	55	ns
→ Output enable to output in low impedance state	t_{OLZ}	5	—	10	—	ns
→ Output to output in high impedance state	t_{CHZ}	0	40	0	40	ns
Chip disable to output in high impedance state	t_{OHZ}	0	40	0	40	ns
→ Output hold from address change	t_{OH}	5	—	10	—	ns
Write cycle						
Write cycle time	t_{WC}	100	—	120	—	ns
→ Chip select to end of write	t_{CW}	90	—	100	—	ns
→ Address valid to end of write	t_{AW}	100	—	105	—	ns
→ Address set-up time	t_{AS}	20	—	20	—	ns
→ Write pulse width	t_{WP}	80	—	85	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high impedance state	t_{OHZ}	0	40	0	40	ns
→ Write to output in high impedance state	t_{WHZ}	0	40	0	40	ns
Data-to-write time overlap	t_{DW}	30	—	35	—	ns
Data hold from write time	t_{DH}	5	—	5	—	ns
→ Output active from end of write	t_{OW}	5	—	5	—	ns

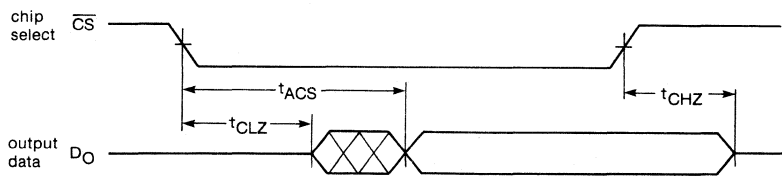


(a) Read cycle 1

DEVELOPMENT DATA



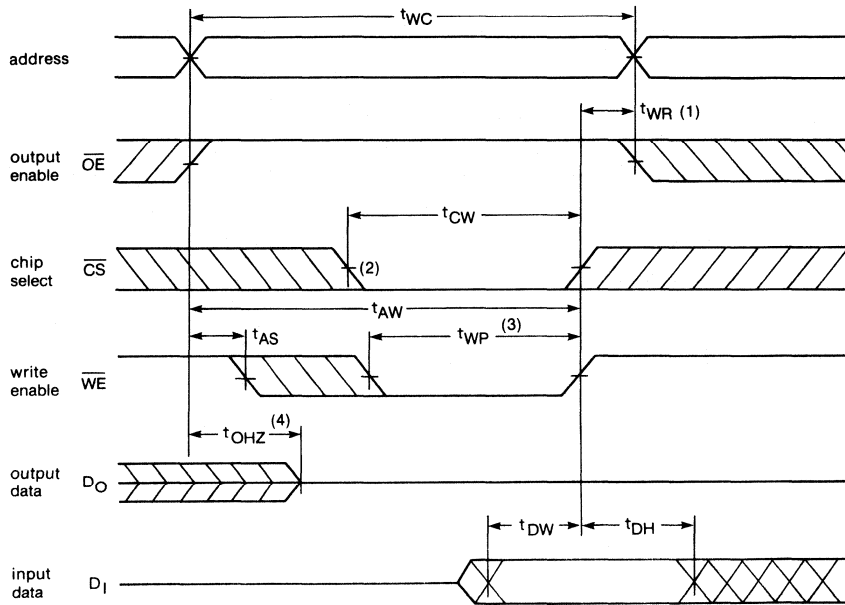
(b) Read cycle 2: device is continuously selected ($\overline{CS} = V_{IL}$); $\overline{OE} = V_{IL}$



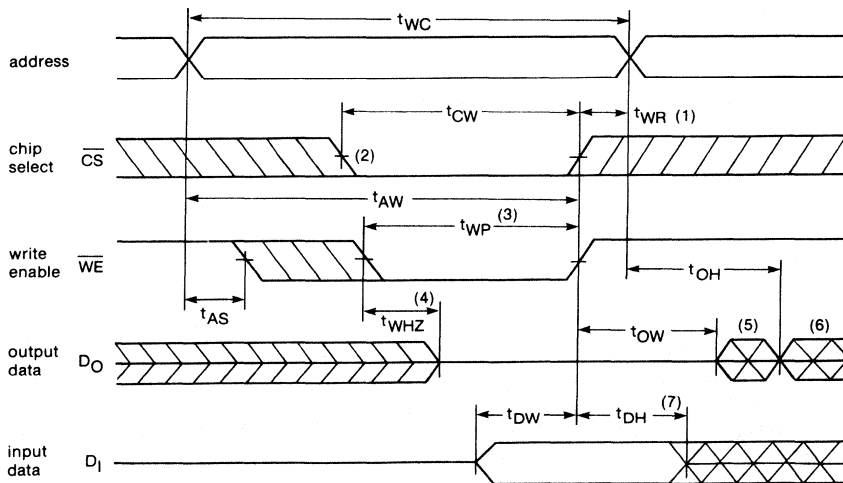
7Z80794

(c) Read cycle 3: address valid prior to or coincident with \overline{CS} transition LOW; $\overline{OE} = V_{IL}$

Fig. 4 Read cycle timing: \overline{WE} is HIGH for a read cycle; when \overline{CS} is LOW the address input must not be left floating.



(a) Write cycle 1



7Z80795

(b) Write cycle 2: $\overline{OE} = V_{IL}$

Fig. 5 Write cycle timing: \overline{WE} must be HIGH during all address transitions.

Notes to Fig. 5

1. t_{WR} is measured from \overline{CS} or \overline{WE} transition HIGH, whichever is the earlier, to the address change.
2. t_{WHZ} is measured under the condition $\overline{CS} = \text{LOW}$.
3. A write occurs during the overlap (t_{WP}) of $\overline{CS} = \text{LOW}$ and $\overline{WE} = \text{LOW}$.
4. During this period, I/O pins are in the output state and input signals of the opposite phase to the outputs must not be applied.
5. D_O has the same phase as write data of this write cycle.
6. D_O is the read data of the next address.
7. If \overline{CS} is LOW during this period, I/O pins are in the output state and input signals of the opposite phase to the outputs must not be applied.

DATA RETENTION CHARACTERISTICS FOR LOW POWER/STANDBY MODE (Fig. 6)

$T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage V_{CC} for data retention at $C_S \geq V_{CC} - 0,2 \text{ V};$ $V_I \geq V_{CC} - 0,2 \text{ V or } \leq 0,2 \text{ V}$	V_{DR}	2,0	—	—	V
Supply current during data retention at $V_{DR} = 3,0 \text{ V}; \overline{CS} \geq 2,8 \text{ V};$ $V_I \geq -0,5 \text{ V}$	I_{DR}	—	—	50	μA
Timing					
Chip deselect to data retention time	t_{CDR}	0	—	—	ns
Recovery time to fully active	t_R	t_{RC}^*	—	—	ns

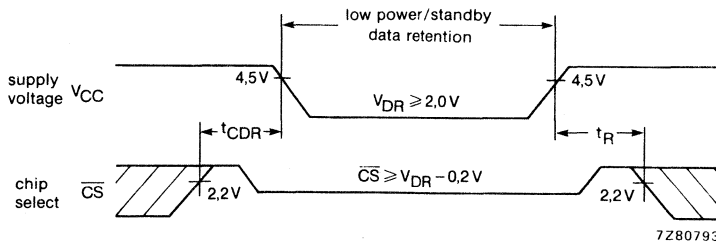


Fig. 6 Data retention waveform.

* t_{RC} = read cycle time.

CMOS EEPROM

PCB8582 2048-bit static EEPROM (256 x 8)113



STATIC CMOS EEPROM (256 x 8 BIT)

GENERAL DESCRIPTION

The PCB8582 is a 2K-bit 5 V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C bus, an eight pin DIL package is sufficient. Up to eight PCB8582 devices may be connected to the I²C bus.

Chip select is accomplished by three address inputs.

Features

- Non-volatile storage of 2K-bit organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10 000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572



PACKAGE OUTLINE

PCB8582P: 8-lead DIL; plastic (SOT-97AE).



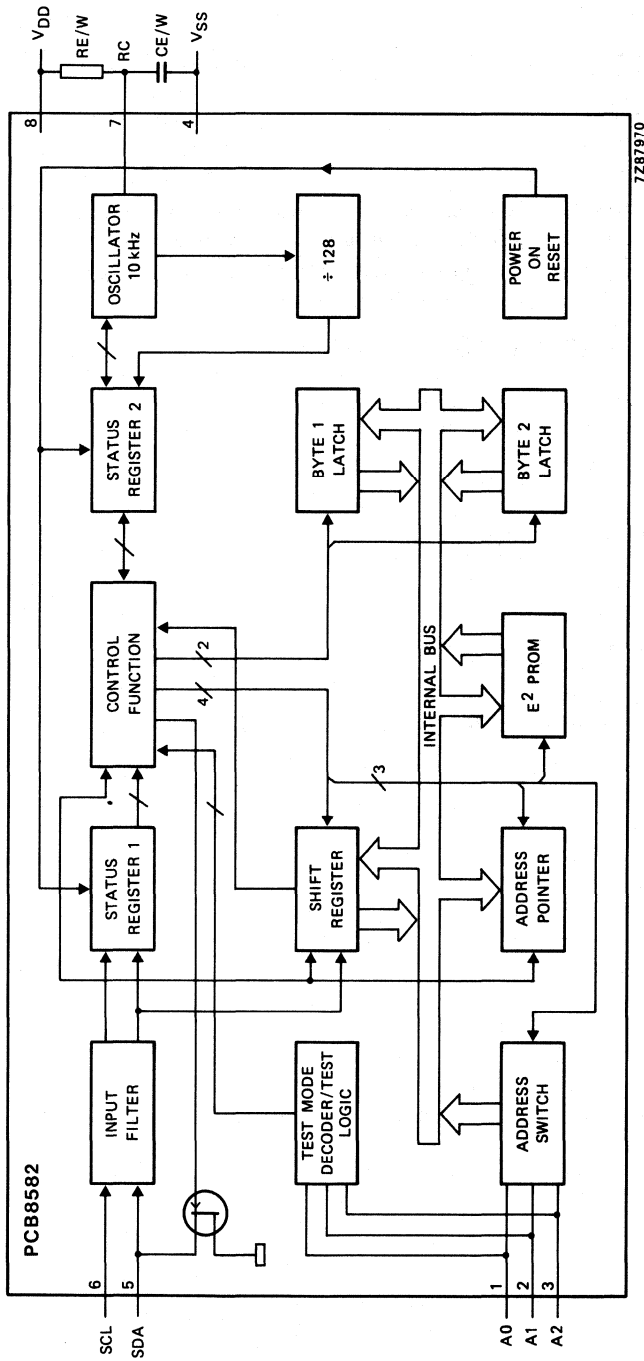


Fig. 1 Block diagram.

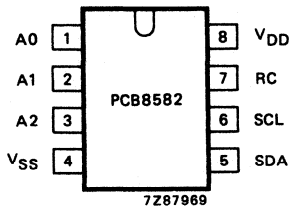


Fig. 2 Pinning diagram.

- 1 A0
- 2 A1 address inputs/test
- 3 A2 mode select
- 4 VSS ground
- 5 SDA } I²C bus lines
- 6 SCL }
- 7 RC input for timer constant
- 8 VDD positive supply

FUNCTIONAL DESCRIPTION

Characteristics of the I²C bus

The I²C bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C bus specifications a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The PCB8582 works in both modes.

By definition a device that gives out a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.

Set-up-and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVELOPMENT DATA

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

I²C bus protocol

The I²C bus configuration for different READ and WRITE cycles of the PCB8582 are shown in Fig. 3, (a) and (b).

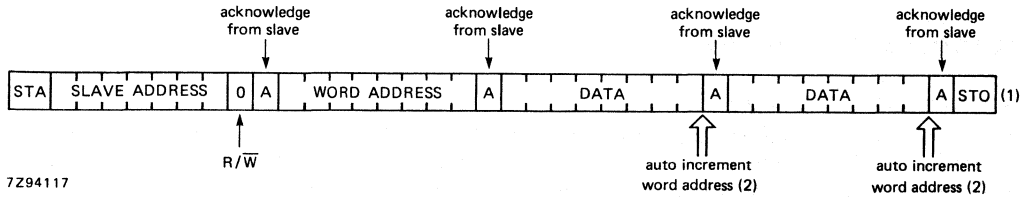


Fig. 3(a) Slave receiver ERASE/WRITE mode.

1. After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximately 20 ms if only one byte is written, and 40 ms, if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via I²C bus.
2. The second data byte is voluntary. Trying to erase/write more than two bytes is not allowed.

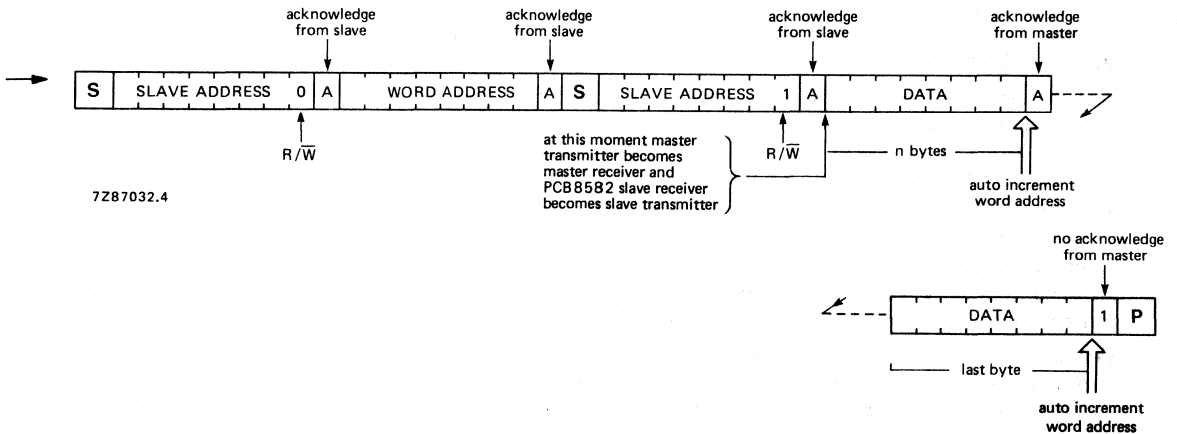
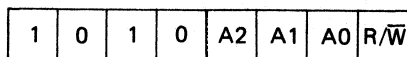


Fig. 3(b) Master reads PCB8582 slave after setting word address. (WRITE word address; READ data).

→ **Note:** The slave address is defined in accordance with the I²C bus specification as:



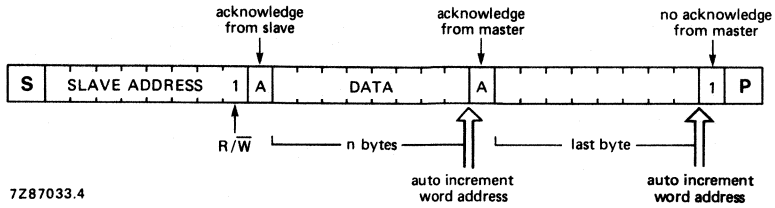


Fig. 3(c) Master reads PCB8582 slave immediately after first byte (READ mode).

I²C bus timing

Fig. 4 shows the I²C bus timing.

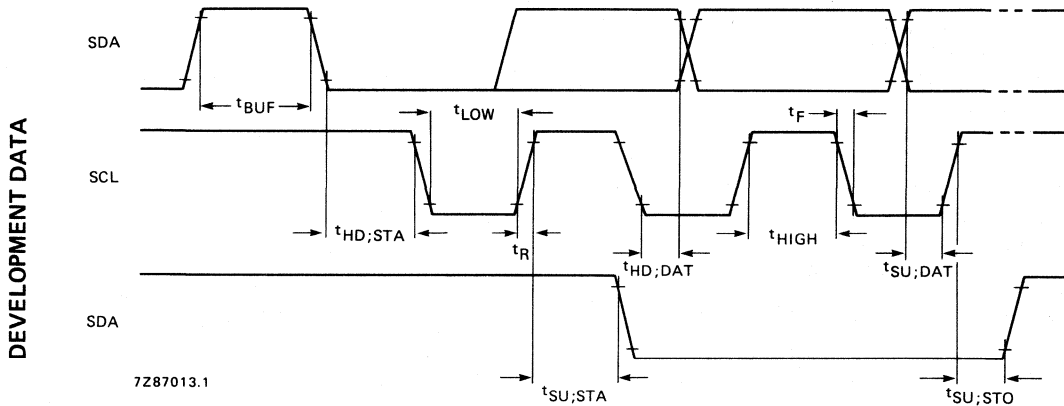


Fig. 4 Timing requirements for the I²C bus.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V _{DD}	-0,3 to 7 V
Voltage, on any input pin (input impedance 500 Ω)	V _I	V _{SS} -0,8 to V _{DD} +0,8 V
Operating temperature range	T _{amb}	0 to +70 °C
Storage temperature range	T _{stg}	-65 to +150 °C
Current into any input pin	I _I	1 mA
Output current	I _O	10 mA

CHARACTERISTICS

→ $V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 0\text{ to }+70\text{ }^{\circ}\text{C}$, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5	5,5	V
Operating supply current, READ ($f_{SCL} = 100\text{ kHz}$)	I_{DDR}	—	0,1	—	mA
Operating supply current, WRITE/ERASE	I_{DDW}	—	1	—	mA
Standby supply current ($V_{DD} = 5\text{ V}$)	I_{DDO}	—	5	—	μA
Input SCL					
Input/output SDA:					
Input voltage LOW	V_{IL}	-0,3	—	1,5	V
Input voltage HIGH	V_{IH}	3	—	$V_{DD}+0,8$	V
Output voltage LOW ($I_{OL} = 3\text{ mA}$, $V_{DD} = 4,5\text{ V}$)	V_{OL}	—	—	0,4	V
Output leakage current HIGH ($V_{OH} = V_{DD}$)	I_{OH}	—	—	1	μA
Input leakage current (A0,A1,A2, SCL), (note 1)	$\pm I_{IN}$	—	—	1	μA
Clock frequency	f_{SCL}	0	—	100	kHz
Input capacity (SCL,SDA)	C_I	—	—	7	pF
Noise suppression time constant at SCL and SDA input	t_I	0,25	0,5	1	μs
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	—	—	μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4	—	—	μs
The LOW period of the clock	t_{LOW}	4,7	—	—	μs
The HIGH period of the clock	t_{HIGH}	4	—	—	μs
Set-up time for start condition (only relevant for a repeated start condition)	$t_{SU;STA}$	4,7	—	—	μs
Hold time DATA for:					
CBUS compatible masters	$t_{HD;DAT}$	5	—	—	μs
I ² C devices (note 2)	$t_{HD;DAT}$	0	—	—	μs
Set-up time DATA	$t_{SU;DAT}$	250	—	—	ns
Rise time for both SDA and SCL lines	t_R	—	—	1	μs
Fall time for both SDA and SCL lines	t_F	—	—	300	ns
Set-up time for stop condition	$t_{SU;STO}$	4,7	—	—	μs
Erase/write timer constant (note 3)					
Erase/write cycle time	$t_{E/W}$	20	—	100	ms
Erase/write timing capacitor for erase/write cycle of 30 ms	$C_{E/W}$	—	3,3	—	nF
Erase/write timing resistor for erase/write cycle of 30 ms	$R_{E/W}$	—	56	—	k Ω
Data retention time	t_S	10	—	—	years

Notes to the characteristics

1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD} .
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300 ns) of the falling edge of SCL.
3. Endurance (number of erase/write cycles), NE/W, is 10^4 E/W cycles.



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Charge—Coupled Memory

SAA9001	317K-bit CCD memory	123
---------	---------------------------	-----

317K-BIT CCD MEMORY

GENERAL DESCRIPTION

The SAA9001 is a 1-bit wide, 317,520 bits long charge-coupled shift register, organized in 294 blocks of 1080 bits each. It is intended for use in a tv field memory at a maximum frequency of 21,3 MHz.

The IC is encapsulated in a 28-pin dual-in-line package of which only fifteen pins are used. Power supplies of +5 and -3,5 V are required. All inputs, outputs and controls are TTL-compatible.

Control is performed by two external signals, memory clock (MC) and memory gating (MG). The circuit has two data inputs (MI₁ and MI₂) and the data may be internally recirculated. An adjustable delay of 0 to 7 bits is incorporated at the output to increment the total delay on a bit-by-bit basis, as programmed by the inputs A0, A1 and A2.

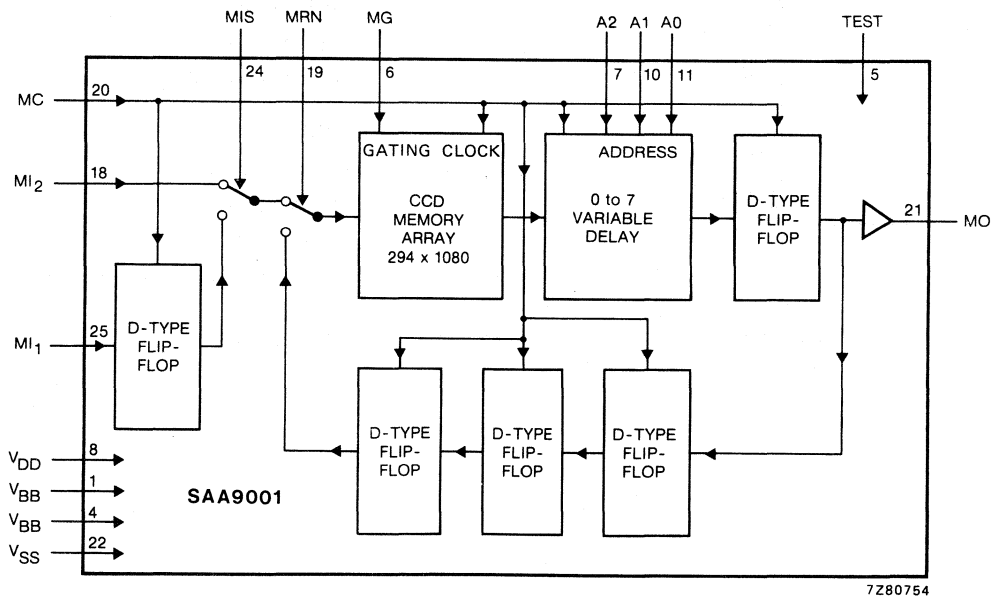


Fig. 1 Block diagram.

PACKAGE OUTLINES

SAA9001PB: 28-lead DIL; plastic (SOT-117).

SAA9001EB: 28-lead DIL; metal ceramic (cerdil) (SOT-87B).

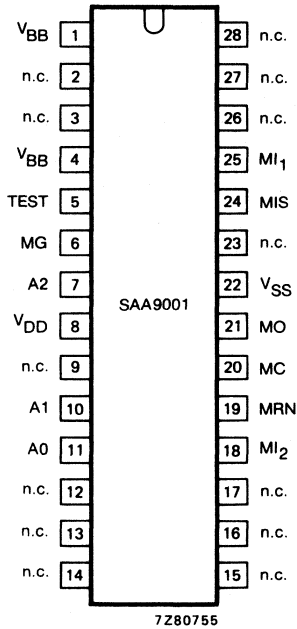


Fig. 2 Pinning diagram.

PINNING

- | | | |
|----|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | V _{BB} | back-bias supply voltage (to be connected to pin 4) |
| 4 | V _{BB} | back-bias supply voltage (to be connected to pin 1) |
| 5 | TEST | control input for testing purposes only. It is internally connected to V _{SS} via a 1 kΩ (approx.) resistor and needs no external connection |
| 6 | MG | memory gating input |
| 7 | A2 | control input for additional internal delay |
| 8 | V _{DD} | positive supply voltage |
| 10 | A1 | control input for additional internal delay |
| 11 | A0 | control input for additional internal delay |
| 18 | MI ₂ | memory input-2 |
| 19 | MRN | memory recirculate control. Recirculation is activated when MRN is LOW |
| 20 | MC | memory clock input |
| 21 | MO | memory output |
| 22 | V _{SS} | negative supply voltage (ground) |
| 24 | MIS | memory input select; selects MI ₁ or MI ₂ |
| 25 | MI ₁ | memory input-1 |

FUNCTIONAL DESCRIPTION

Operation

The memory array is organized to handle data in blocks of 1080 bits and has a capacity of 294 data blocks. The structure of the memory array provides fast, serial data input and output, with parallel transfer of data blocks through the memory. Memory input and output are controlled by the memory gating (MG), the serial output being initiated by the rising edge of MG and the storage of the data present in the memory's input register is performed on the falling edge of MG. In normal operation one cycle of MG is an uninterrupted HIGH level of at least 1080 clock periods (-4 or $+3$ clock periods) followed by a LOW level of at least 32 clock periods. Input, output and gating signals are all referred to the rising edge of the memory clock (MC).

The internal recirculation facility is activated when the control input MRN is LOW.

Memory output

Output is enabled when MG is HIGH and data is clocked serially from the memory. Referring to Fig. 3, the first rising clock-edge after the positive transition of MG is defined as clock pulse "0". If the delay control address is $A2 = A1 = A0 = 0$, then the first bit of the output is valid at clock pulse "17" (the delay of 17 clock periods is due to internal multiplexing of the data in the memory).

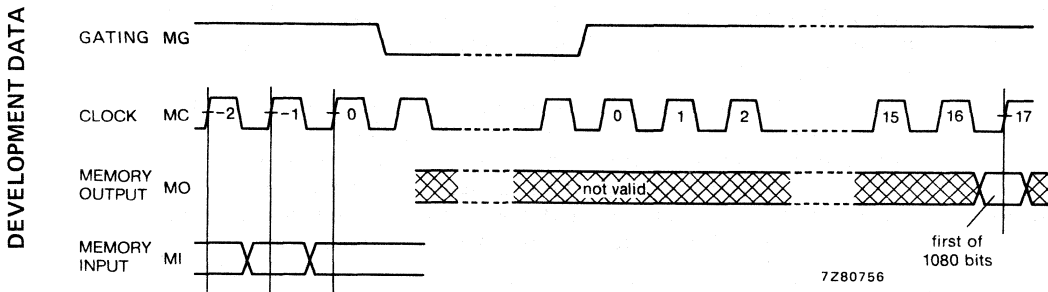


Fig. 3 Memory input and output data timings with respect to the memory clock (MC) for a memory gating (MG) HIGH period that is a multiple of 8 clock periods (no internal rounding of gating period).

The output delay can be increased by the values shown in Table 1 using the internal delay line controlled by A0, A1 and A2.

Table 1 Additional delay control

delay address			additional delay (clock periods)
A2	A1	A0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FUNCTIONAL DESCRIPTION (continued)

Data input

Data to be stored is directed to the memory from either MI_1 or MI_2 as selected by the control input MIS (see Table 2). The MI_1 input is delayed by one clock period.

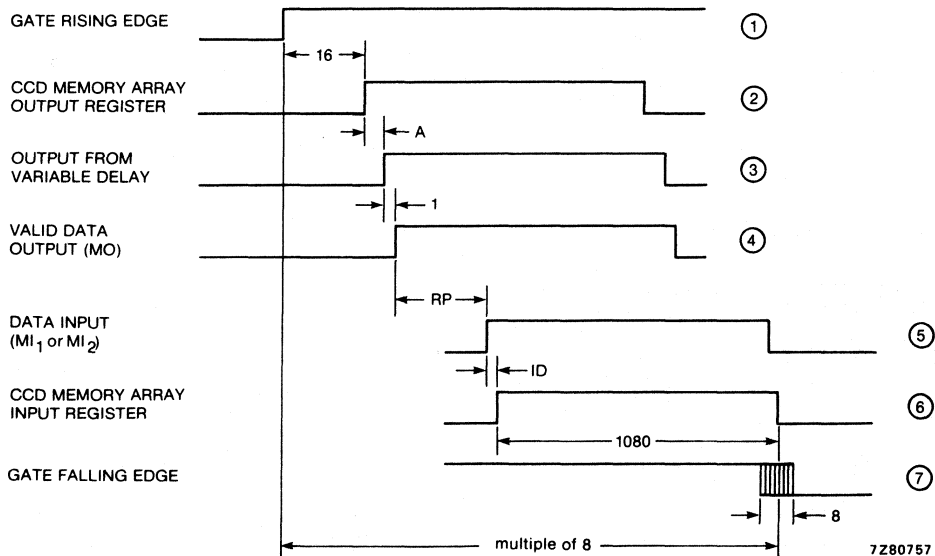
Table 2 Input selection

control input	memory input
MIS = 0	MI_1
MIS = 1	MI_2

Input data is clocked serially into the input register of the CCD memory. When the negative transition of MG occurs, the 1080 bits of data present in the input register are entered into the memory array. If the interval of MG = HIGH is not an exact multiple of eight clock periods then the timing of the negative transition of MG is internally rounded to be an exact multiple of eight clock periods. Note that the data path from input MI_1 has a delay of one clock period and the path from MI_2 is direct.

The length of the MG = HIGH interval required for internal and external recirculation of data is determined as shown in Fig. 4. The positive transition of MG (waveform 1) initiates the serial transfer of data from the output register. Due to multiplexing in the memory, valid data is available after 16 clock periods (waveform 2). After a delay of "A" clock periods, determined by A0, A1 and A2 (waveform 3), and a one-clock-period delay via a D-type flip-flop, the valid data is available at the output pin MO (waveform 4).

Incoming data can be delayed by two amounts: RP (waveform 5), a phase shift introduced when the data is recirculated through an external processing circuit; and ID (waveform 6), a one-clock-period delay when input MI_1 is selected. The negative transition of MG, internally rounded to a multiple of eight clock periods (waveform 7), initiates storage of the last 1080 bits presented at the memory input (waveform 6). Therefore, the MG = HIGH interval is $16 + A + 1 + RP + ID + 1080$ clock periods, and this figure is rounded to a multiple of eight. From this, $(A + 1 + RP + ID) \text{ modulo } 8 = 0$.



7280757

Fig. 4 Determination of memory gating HIGH period.

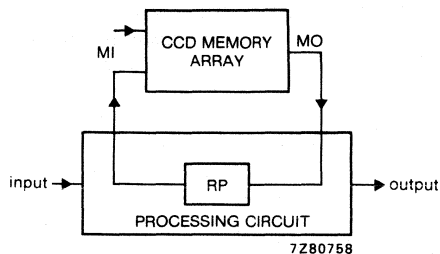


Fig. 5 Recirculation via an external circuit.

During internal recirculation of the data (MRN = LOW), the three D-type flip-flops in the recirculation path give RP a value of three clock periods and ID will be zero. Consequently, the variable delay should be programmed for a delay of $A = 4$ for proper data retention, i.e. $(4 + 1 + 3 + 0) \text{ modulo } 8 = 0$.

In conclusion, to store 1080 bits of valid data and to retrieve at the output 1080 valid data bits, the MG = HIGH interval must be at least 1076 clock periods followed by an MG = LOW interval of at least 32 clock periods. The MG = LOW interval can be reduced to a minimum of 24 clock periods when MG = HIGH is a multiple of eight clock periods.

Fast gating

Fast gating is a method of accelerating the internal transfer of data through the memory at the expense of valid data and is therefore useful for skipping unwanted data blocks. The MG = HIGH interval for fast gating is less than 1076 clock periods to a minimum of 360 clock periods. If the MG = HIGH interval is a multiple of eight clock periods during fast gating, the MG = LOW interval can be reduced to 24 clock periods (min.), otherwise the MG = LOW interval must be at least 32 clock periods. The output data is not valid during fast gating and during the first two data blocks at the output after fast gating has ceased. No valid data is clocked into the input register of the CCD memory during fast gating.

Slow gating

The transfer of data can be decelerated by using slow gating. For this, the MG = HIGH or MG = LOW interval is extended to the maximum waiting time (t_{GW}).

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Voltage on any pin, except V_{BB} (pin 4) and MO (pin 21),
with respect to V_{SS}

V_I, V_O max. 7 V

Back-bias voltage

V_{BB} min. -7 V

D.C. output current (sink or source)

I_O max. 10 mA

Operating ambient temperature range
(under d.c. operating conditions)

T_{amb} 0 to 60 °C

Storage temperature range

T_{stg} -65 to 150 °C

Total power dissipation per package

P_{tot} 1 W

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CAPACITANCE

parameter	symbol	max.	unit
Capacitance at:			
data inputs MI ₁ , MI ₂ (pins 25 and 18)	C _I	9	pF
clock input MC (pin 20)	C _C	9	pF
gating input MG (pin 6)	C _G	9	pF
data output MO (pin 21)	C _O	9	pF
recirculation control MRN (pin 19)	C _{RN}	9	pF
input select control MIS (pin 24)	C _{IS}	9	pF
delay program inputs A0, A1, A2 (pins 11, 10 and 7)	C _A	9	pF

D.C. OPERATING CONDITIONS

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V _{DD}	4,75	—	5,25	V
Back-bias supply range	V _{BB}	-3,65	—	-3,35	V
Input voltage LOW	V _{IL}	-1,0	—	+0,8	V
Input voltage HIGH	V _{IH}	2,0	—	6,0	V

D.C. CHARACTERISTICS

T_{amb} = 0 to + 60 °C; V_{DD} = 4,75 to 5,25 V; V_{BB} = -3,5 ± 0,15 V; output not loaded; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input leakage current at V _i = GND to V _{DD} : MI ₁ ; MI ₂ ; MC; MG; A0; A1; A2; MRN; MIS	I _{LI}	—	—	10	μA
Power supply current from V _{DD} at f = 21,3 MHz	I _{DD}	—	—	70	mA
Output voltage LOW at I _{OL} = 4 mA	V _{OL}	—	—	0,4	V
Output voltage HIGH at I _{OH} = -1 mA	V _{OH}	2,4	—	—	V

A.C. TEST CONDITIONS

Input pulse levels	0,6 and 2,4	V
Rise and fall times between 0,8 and 2,0 V (t_r , t_f)		
clock input MC	≤ 3	ns
data inputs MI ₁ , MI ₂ ; gating input MG; control inputs A0, A1, A2, MIS, MRN	≥ 3	ns
Timing reference levels		
clock input MC	1,5	V
data inputs MI ₁ , MI ₂ and gating input MG	0,8 or 2,0	V
data output MO	0,8 or 2,0	V
Output load	see Fig. 6	

A.C. CHARACTERISTICS

$T_{amb} = 0$ to 60 °C; $V_{DD} = 4,75$ to $5,25$ V; $V_{BB} = -3,5 \pm 0,15$ V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Clock frequency (note 1)	f _{CL}	—	—	21,3	MHz
Clock LOW time	t _{CL}	18	—	—	ns
Clock HIGH time	t _{CH}	18	—	—	ns
Recirculation time (note 1)	t _R	—	—	27	ms
Waiting time (gating LOW/HIGH time) (note 2)	t _{GW}	—	—	1100	μ s
Gating set-up time	t _{GC}	7,5	—	—	ns
Gating hold time	t _{CG}	0,5	—	—	ns
Data set-up time	t _{IC}	7,5	—	—	ns
Data hold time	t _{CI}	0,5	—	—	ns
Output hold time	t _{OH}	5,0	—	—	ns
Output delay time	t _{OD}	—	—	23,5	ns
Output invalid after address change	t _{AH}	0	—	—	μ s
Address valid after address change (note 3)	t _{AD}	—	—	7 clock pulses + 1	μ s
Recirculation set-up time (note 4)	t _{MRNSU}	0	—	1	μ s
Input select set-up time (note 5)	t _{MISSU}	0	—	1 clock pulse + 1	μ s

Notes to the characteristics

1. The maximum recirculation time must never be exceeded by any combination of low frequency gating and/or waiting time.
2. Every 1300 μ s at least three blocks of 1080 bits must be transferred to the output. This means that immediately after a wait of 1100 μ s three blocks must be shifted out.
3. A change in delay will cause invalid data at the output for the time t_{AD}.
4. After a change of MRN, the signal recirculation path is not switched before t_{MRNSU}.
5. After a change of MIS, data at the input is invalid for t_{MISSU}.

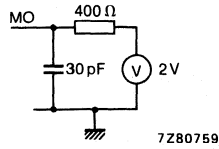


Fig. 6 Output load.

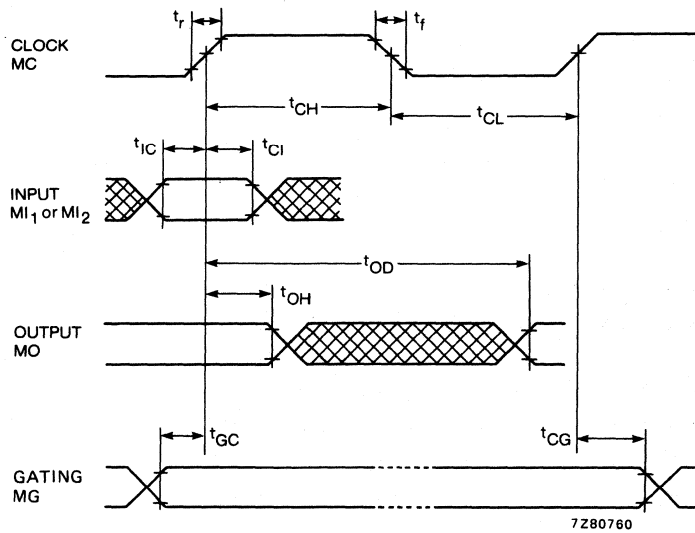


Fig. 7 Timing waveforms for gating and I/O.

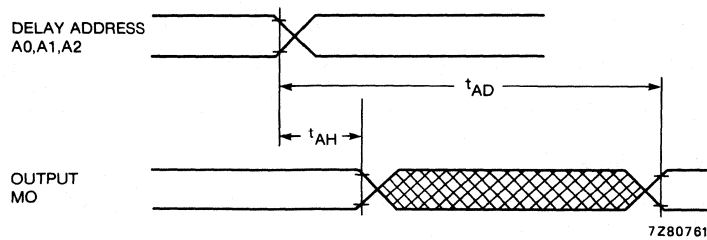


Fig. 8 Timing waveforms for address set-up and hold.

TTL MEMORIES

Introduction	133
64-bit RAM	147
256-bit RAM	157
Byte-Organized RAM	175
PROM Programming Information	195
Low Complexity PROM	199
4K-bit PROM	225
8K-bit PROM	241
16K-bit PROM	271
32K-bit PROM	283
64K-bit PROM	291

Introduction

Quality and Reliability	134
Selection Guide	140
PROM Cross Reference Guide.....	142
RAM Cross Reference Guide.....	144
Ordering Information	145

Bipolar Memory Products

SIGNETICS' BIPOLAR MEMORY QUALITY

Signetics has put together a winning process for manufacturing Bipolar Memories. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The memories produced in the Standard Products Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 amps/cm². Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data

also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from -55°C to +125°C and at +10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 — QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Bipolar Memory prod-

ucts, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: $T_J = 150^\circ\text{C}$, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: $T_J = 150^\circ\text{C}$, 1000 hours
- Temperature Humidity Biased Life: 85°C , 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): -65°C to $+150^\circ\text{C}$, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C , 100% saturated steam) and 300 cycles of thermal shock (-65°C to $+150^\circ\text{C}$)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality and Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the bipolar memory SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors
- Device or generic group failure rate studies
- Advanced environmental stress development
- Failure mechanism characterization and corrective action/prevention reporting

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership*.

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100ppm (parts per million), down from an industry practice of 10,000ppm, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented

low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

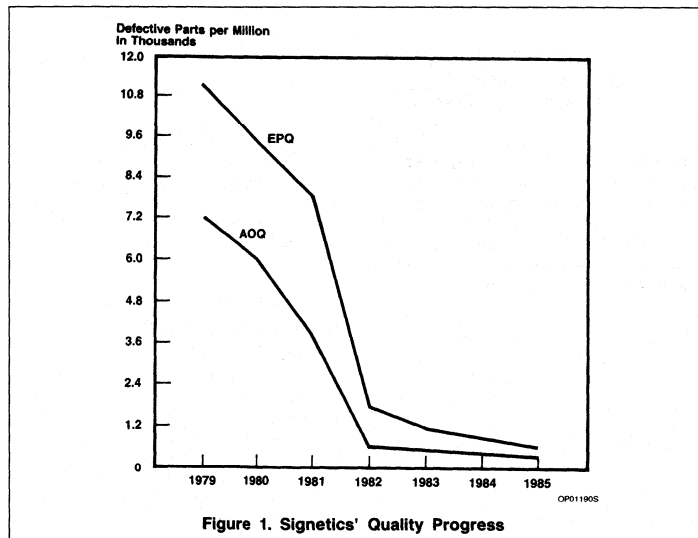


Figure 1. Signetics' Quality Progress

Quality and Reliability

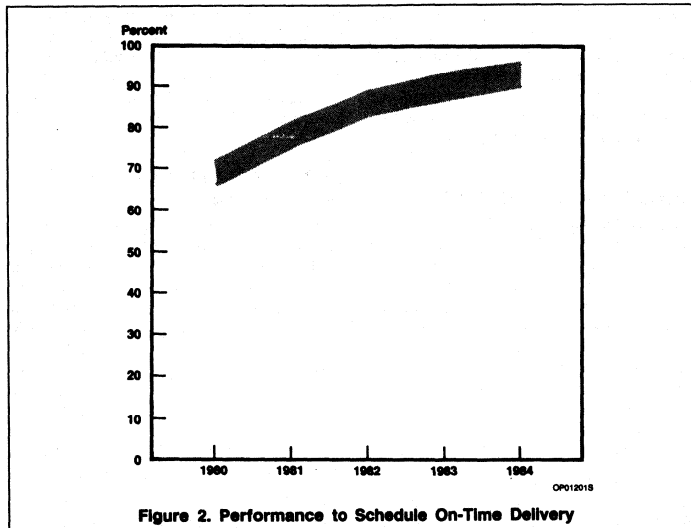


Figure 2. Performance to Schedule On-Time Delivery

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed-upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The quality improvement program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" — ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to

the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

PRODUCT QUALITY PROGRAM

To reduce defects in outgoing products, we created the Product Quality Program. This is managed by the Product Engineering Council, composed of the top product engineering and test professionals in the company. This group:

1. Sets aggressive product quality improvement goals;
2. provides corporate-level visibility and focus on problem areas;
3. serves as a corporate resource for any group requiring assistance in quality improvement; and
4. drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Quality and Reliability

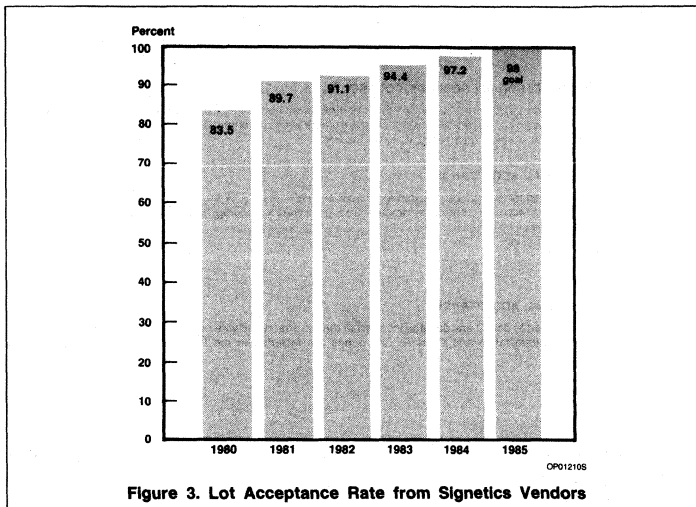


Figure 3. Lot Acceptance Rate from Signetics Vendors

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

MATERIAL WAIVERS

1985 - (0) (Goal)
 1984 - 0
 1983 - 0
 1982 - 2
 1981 - 134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions:

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities — failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the corporate director of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. During the development of the program many profound changes were made. Figure 4, *Bipolar Memory Process Flow*, shows the result. Key changes included such things as implementing 100% temperature testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading quality supplier of bipolar memories. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

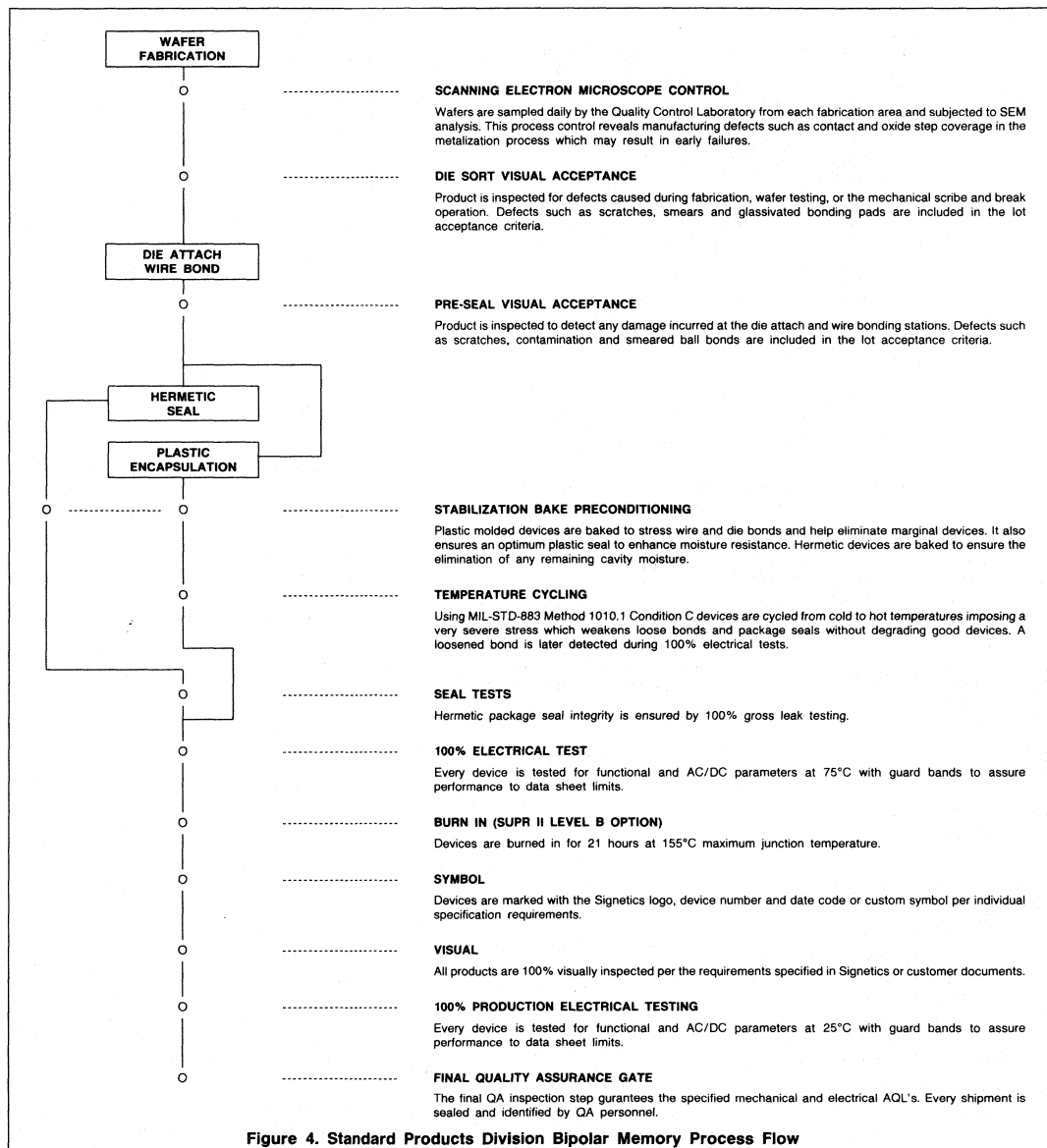
OUR GOAL: 100% PROGRAMMING YIELD

Our original goal back in the early 1970s was to develop a broad line of programmable products which would be recognized as having the best programming yield in the industry. Within the framework of a formal quality program, our efforts to improve circuit designs and refine manufacturing controls have resulted in major advances toward that goal.

Also within the framework of our formal quality program, we have now established a stated goal of 100% programming yield. Through the increasing effectiveness of a quality attitude of "Do It Right The First Time" we're moving ever closer to that target.

A significant amount of data on programming yields has been collected over the past two years. This data is the result of both inhouse programming (customer orders) and reports from major users of fuseable products. The data covers the full range of products from 256-bit PROMs to 64K PROMs and indicates an average level of 97.7% programming yield.

Quality and Reliability



Quality and Reliability

As time goes on the drive for a product line that has Zero Defects will grow in intensity. These efforts will provide both Signetics and our customers with the ability to achieve the mutual goal of improved product quality.

The Bipolar Memory Quality Assurance department has monitored ppm progress, which can be seen in Figure 5. We are pleased with the progress that has been made, and expect to achieve even more impressive results as the procedures for accomplishing these tasks are fine tuned.

The real measure of any quality improvement program is the result that our customers see. The meaning of *Quality* is more than just working circuits. It means commitment to *On Time Delivery at the Right Place of the Right Quantity of the Right Product at the Agreed Upon Price.*

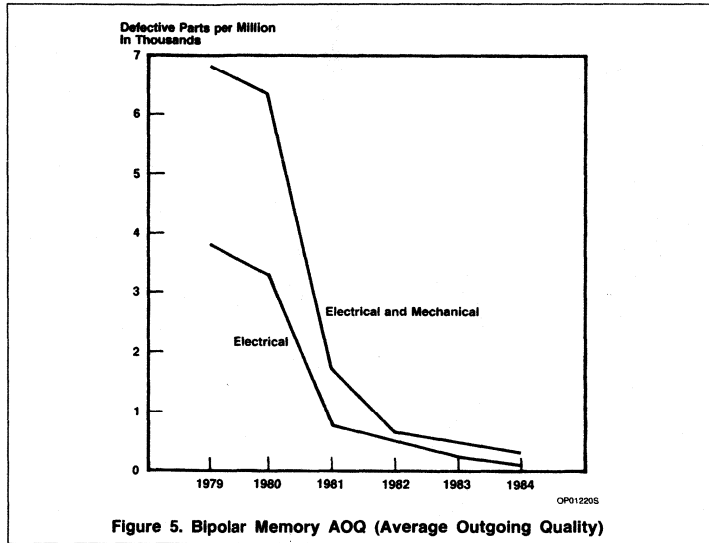


Figure 5. Bipolar Memory AOQ (Average Outgoing Quality)

Bipolar Memory Products

DEVICE ⁵	ORGANIZATION	OUTPUT CIRCUIT ¹	OUTPUT LOGIC ²	ACCESS TIME ³	PACKAGE ⁴	PINS	MAX I _{CC}
RAMs							
82S25	16 × 4	OC	B	50	N	16	105
3101A	16 × 4	OC	B	35	N	16	105
74S189	16 × 4	TS	B	35	N	16	110
74F189	16 × 4	TS	B	20	N	16	100
82S16	256 × 1	TS	T	50	N	16	115
74S301	256 × 1	OC	B	50	N	16	130
82LS16	256 × 1	TS	T	40	N	16	70
74LS301	256 × 1	OC	B	40	N	16	70
82S09	64 × 9	OC	T	45	A, N	28	190
82S09A	64 × 9	OC	T	35	A, N	28	190
82S19	64 × 9	OC	B	35	N	28	190
82S212	256 × 9	TS	B	45	N	22	185
82S212A	256 × 9	TS	B	35	N	22	185
8X350	256 × 8	TS	B	N/A	N	22	185
PROMs							
82S23	32 × 8	OC	—	50	N	16	96
82S23A	32 × 8	OC	—	25	D, N	16	96
82S23B ⁶	32 × 8	OC	—	15	D, N	16	110
82S123	32 × 8	TS	—	50	N	16	96
82S123A	32 × 8	TS	—	25	D, N	16	96
82S123B ⁶	32 × 8	TS	—	15	D, N	16	110
82S126	256 × 4	OC	—	50	N	16	120
82S126A	256 × 4	OC	—	30	D, N	16	120
82S129	256 × 4	TS	—	50	N	16	120
82S129A	256 × 4	TS	—	27	D, N	16	120
10149	256 × 4	OE	—	20	F	16	150
100149	256 × 4	OE	—	20	F	16	150
82S130	512 × 4	OC	—	50	D, N	16	140
82S130A	512 × 4	OC	—	33	D, N	16	140
82S131	512 × 4	TS	—	50	N	16	140
82S131A	512 × 4	TS	—	30	D, N	16	140
82LS135	256 × 8	TS	—	100	D, N	20	100
82S135	256 × 8	TS	—	45	D, N	20	150
82S115	512 × 8	TS	—	60	N	24	175
82S137	1024 × 4	TS	—	60	N	18	140
82S137A	1024 × 4	TS	—	45	D, N	20, 18	140
82S137B	1024 × 4	TS	—	35	D, N	20, 18	140
82S147	512 × 8	TS	—	60	D, N	20	155
82S147A	512 × 8	TS	—	45	D, N	20	155
82LS181	1024 × 8	TS	—	120	A, N	24	80
82S181	1024 × 8	TS	—	70	N	24	175
82S181A	1024 × 8	TS	—	55	A, N	28, 24	175
82S181C	1024 × 8	TS	—	30	A, N, N3	28, 24	175
82S183	1024 × 8	TS	—	60	N	24	175
82S185	2048 × 4	TS	—	100	N	18	120
82S185A	2048 × 4	TS	—	50	D, N	20, 18	155
82S185B	2048 × 4	TS	—	45	D, N	20, 18	155
82HS187	1024 × 8	TS	R	55	N	24	155
82HS187A	1024 × 8	TS	R	45	N	24	155
82HS189	1024 × 8	TS	R	55	N	24	155
82HS189A	1024 × 8	TS	R	45	N	24	155

Selection Guide

DEVICE ⁵	ORGANIZATION	OUTPUT CIRCUIT ¹	OUTPUT LOGIC ²	ACCESS TIME ³	PACKAGE ⁴	PINS	MAX I _{cc}
PROMs							
82S191	2048 × 8	TS	—	80	N	24	175
82S191A	2048 × 8	TS	—	55	N	24	175
82S191C	2048 × 8	TS	—	35	A, N, N3	24	175
82HS195	4096 × 4	TS	—	45	N	20	145
82HS195A	4096 × 4	TS	—	35	N	20	145
82HS195B	4096 × 4	TS	—	25	N	20	145
82HS197 ⁶	2048 × 8	TS	R	65	N	24	155
82HS199 ⁶	2048 × 8	TS	R	65	N	24	155
82S321	4096 × 8	TS	—	70	N	24	175
82HS321	4096 × 8	TS	—	45	N	24	175
82HS321A	4096 × 8	TS	—	35	N	24	175
82HS321B	4096 × 8	TS	—	30	N	24	175
82HS641	8192 × 8	TS	—	55	N	24	175
82HS641A	8192 × 8	TS	—	45	N	24	175
82HS641B	8192 × 8	TS	—	35	N	24	175
82HS1281 ⁶	16384 × 8	TS	—	45	N	24	175

NOTES:

1. Output circuit

- OE = Open Emitter
- OC = Open Collector
- TS = 3 State

2. Output logic

- T = Transparent — input data appears on output during Write
- B = Blanked — output is blanked during Write
- R = Registers
- I/O = Programmable input/output option

3. Commercial (0°C to +75°C)

4. Packages:

- N = Plastic Dual In Line (N3 = 300 mil wide)
- A = Plastic Square Leaded Chip Carrier
- D = Small Outline Large (SO-L)

*Whenever a single device is offered in both 300 mil wide and 600 mil wide packages, designate either N3 (300 mil) or N (600 mil) to assure proper order entry and shipment.

5. Part numbers:

- 82Sxxx Junction Isolated
- 82HSxxx Oxide Isolated

6. Objective spec (under product development)

Bipolar Memory Products

ORGANIZATION	PKG. PINS	SIGNETICS	MMI	TI	HARRIS*
32 x 8 OC	16	N82S23 N82S23A	6330-1 63S080	18SA030J, N	HM7602-5
32 x 8 TS	16	N82S123 N82S123A	6331-1 63S081	18S030J, N	HM7603-5
256 x 4 OC	16	N82S126 N82S126A	6300-1 63S140	24SA10J, N	HM7610-5 HM7610A-5 HM7610B-5
256 x 4 TS	16	N82S129 N82S129A	6301-1 63S141	24S10J, N	HM7611-5 HM7611A-5 HM7611B-5
256 x 4 OE	16	10149**			
256 x 4 OE	16	100149**			
256 x 8 TS	20	N82S135	6309-1	18S22J, N	
256 x 8 TS	20	N82LS135		28L22J, N	
512 x 4 OC	16	N82S130 N82S130A	6305-1 63S240		HM7620-5 HM7620A-5 HM7620B-5
512 x 4 TS	16	N82S131 N82S131A	6306-1 63S241		HM7621-5 HM7621A-5 HM7621B-5
512 x 8 TS	20	N82S147 N82S147A	6349-1 6349-2	28S42J, N	HM7648-5 HM7649A-5
512 x 8 TS	24	N82S141	6341-1	28S46J, N	HM7641-5
512 x 8 TS	24	N82S115			
1024 x 4 TS	18	N82S137 N82S137A N82S137B	6353-1 63S441 63S441A	24S41J, N	HM7643-5 HM7643A-5 HM7643B-5
1024 x 8 TS	24	N82S181 N82S181A N82S181C	6381-1 6381-2 63S881	28S86J, N 28S86-60J, N	HM7681-5 HM7681A-5
1024 x 8 TS	24	N82S181CN3			
1024 x 8 TS	24	N82LS181		28L86J, N	
1024 x 8 TS	24	N82S183			
1024 x 8 TS	24	N82HS187*** N82HS187A***			
1024 x 8 TS	24	N82HS189*** N82HS189A***	63RS881		
2048 x 4 TS	18	N82S185 N82S185A N82S185B	- 63S841	- 24S81J, N 24S81-55J, N	HM7685-5 HM7685A-5
2048 x 8 TS	24	N82S191 N82S191A N82S191C	63S1681	28S166J, N 28S166-55J, N	HM76161-5 HM76161A-5
2048 x 8 TS	24	N82S191CN3	63S168INS		
4096 x 4 TS	20	N82HS195 N82HS195A N82HS195B	63S1641 63S1641A		HM76165-5
4096 x 8 TS	24	N82S321			HM76321-5
4096 x 8 TS	24	N82HS321 N82HS321A N82HS321B	63S3281 63S3281A		
8192 x 8 TS	24	N82HS641 N82HS641A N82HS641B			HM76641-5 HM76641A-5
16384 x 8 TS	28	N82HS1281***			

* Possibly Discontinued Products

** ECL

***Planned New Product

PROM Cross Reference Guide

RAYTHEON	AMD	NATIONAL	FAIRCHILD	MOTOROLA	INTEL
	AM27S18AC	DM74S188			
	AM27S19AC	DM74S288			
29660C*	AM27S20C AM27S20AC	DM74S387	93417C*		3601*
29661C*	AM27S21C AM27S21AC	DM74S287	93427C*		3621*
			F10416**	MCM10149**	
			F100416**		
		DM74LS471			
29610C*	AM27S12C AM27S12AC	DM74S570 DM74S570A	93436C*	MCM7620C	3602* 3602A*
29611C	AM27S13C AM27S13AC	DM74S571 DM74S571A	93446C*	MCM7621C	3622* 3622A*
29621C 29621AC	AM27S29C	DM74S472 DM74S472A			
29625C*	AM27S31C	DM74S474	93448C*	MCM7641C	3624* 3624A*
29641C*	AM27S33C AM27S33AC	DM74S573 DM74S573A DM74S573B	93453C	MCM7643C	3625*
29631C 29631AC	AM27S181C	DM87S181 DM87S181A	93Z451C	MCM7681C	3628*
	AM27S281A	DM87S281A			
			93L451C*		
	AM27S35C AM27S35AC				
	AM27S37C AM27S37AC	DM87SR181			
29651C 29651AC	AM27S185C	DM87S185 DM87S185A	93515C*	MCM7685C	
29681C 29681AC	AM27S191C AM27S191AC	DM87S191 DM87S191A	93Z511C	MCM76161AC	3636B*
	AM27S291C AM27S291M	DM87S291 DM77S291			
	AM27S41C AM27S41AC	DM87S195A DMR7S195B	93513C*		
29671C					3632* 3632-1*
29671AC	AM27S43C AM27S43AC	DM87S321			
	AM27S49C AM27S49AC		93Z565C 93Z565AC		

Bipolar Memory Products

ORGANIZATION	PKG PINS	SIGNETICS	$\frac{T_{AA}}{I_{CC}}$	FAIRCHILD	$\frac{T_{AA}}{I_{CC}}$	TI	$\frac{T_{AA}}{I_{CC}}$	AMD	$\frac{T_{AA}}{I_{CC}}$	NATIONAL	$\frac{T_{AA}}{I_{CC}}$
16 × 4 OC	16	N3101A	$\frac{35}{105}$	93403*	NA	SN74S289A	$\frac{35}{105}$	AM27S02 AM3101A	$\frac{35}{100}$ $\frac{35}{100}$	DM74S289	$\frac{35}{110}$
16 × 4 TS	16	N74S189	$\frac{35}{110}$	93405*	NA	SN74S189A	$\frac{35}{110}$	AM27S03	$\frac{35}{100}$	DM74S189	$\frac{35}{110}$
16 × 4 OS	16	N82S25	$\frac{50}{105}$	93403*	NA	SN74S289A	$\frac{35}{105}$	AM27S02	$\frac{35}{100}$	DM74S289	$\frac{35}{110}$
64 × 9 OC	28	N82S09 N82S09A T	$\frac{45}{190}$ $\frac{35}{190}$								
64 × 9 OC	28	N82S19	$\frac{35}{190}$	93419 93419A	$\frac{45}{150}$ $\frac{35}{150}$						
256 × 1 OC	16	N74S301	$\frac{50}{130}$			SN74S301	$\frac{65}{140}$	AM27LS01A	$\frac{35}{115}$		
256 × 1 OC	16	N74LS301	$\frac{40}{70}$					AM27LS01	$\frac{45}{70}$		
256 × 1 TS	16	N82S16 T	$\frac{50}{115}$	93421* T	NA	SN74S201	$\frac{65}{140}$	AM27LS00-1A T	$\frac{35}{115}$	74S200* T	NA
256 × 1 TS	16	N82LS16 T	$\frac{40}{70}$					AM27LS00-1 T	$\frac{45}{70}$	74S206* T	NA
256 × 8 TS	22	N8X350	$\frac{NA}{185}$								
256 × 9 TS	22	N82S212 N82S212A	$\frac{45}{185}$ $\frac{35}{185}$	93479 93479A	$\frac{45}{185}$ $\frac{35}{185}$						

NOTES:

T: Output is Transparent during write
*: Possibly Discontinued

Bipolar Memory Products

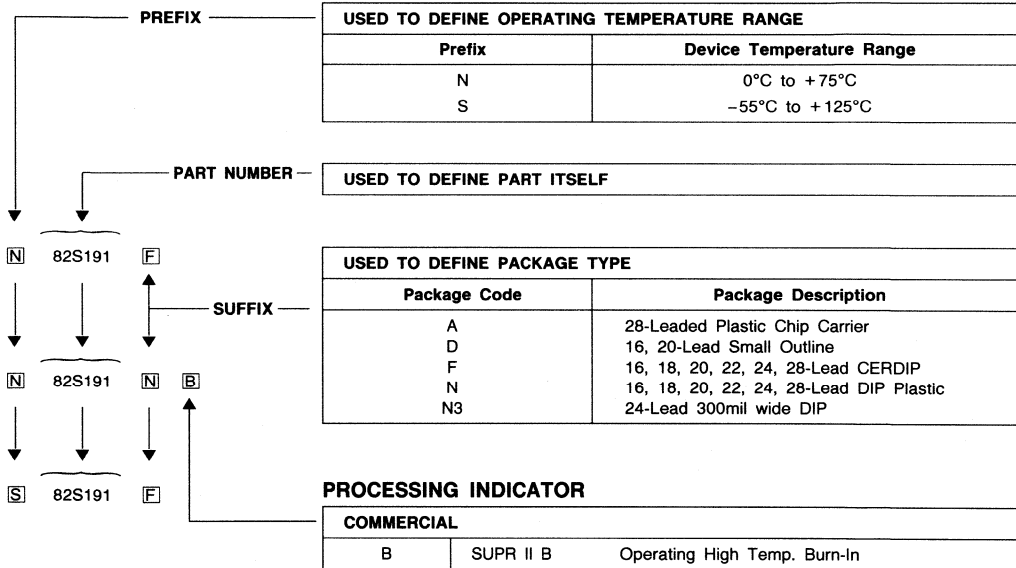
Signetics Bipolar Memory integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

The table shown provides part number definition for Signetics memory products. The Signetics part number system allows complete definition for ordering a device. The part number itself and the product description is defined on each data sheet. The suffix is a single letter defining a package type (as shown in the table on this page). Additional or special

processing is defined by adding the processing indicator when required.

The military qualification, Full MIL Signetics or Full JAN slash sheet status, can be determined by contacting Signetics Military Division or referring to the Signetics Military Data Book.

Table 1. Part Number Description



64-bit TTL Bipolar RAM

82S25/3101A/74S189	64-bit RAM (16 x 4).....	149
74F189	64-bit RAM (16 x 4).....	153

82S25 3101A 74S189 64-Bit TTL Bipolar RAM

Bipolar Memory Products

Product Specification

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature PNP inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

Ordering information can be found on the following page.

The 82S25 and 74S189 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

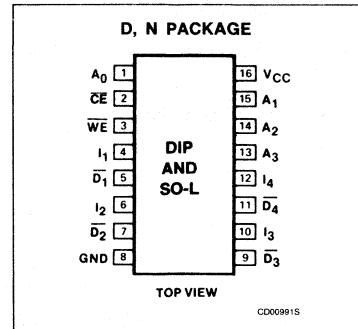
FEATURES

- Output access time:
 - N82S25: 50ns max
 - N3101A: 35ns max
 - N74S189: 35ns max
- Power dissipation: 6.25mW/bit, typ
- Input loading: $-100\mu\text{A}$ max
- On-chip address decoding
- One chip enable input
- Output options:
 - N82S25: Open collector
 - N3101A: Open collector
 - N74S189: Three-state
- Schottky clamped
- TTL compatible

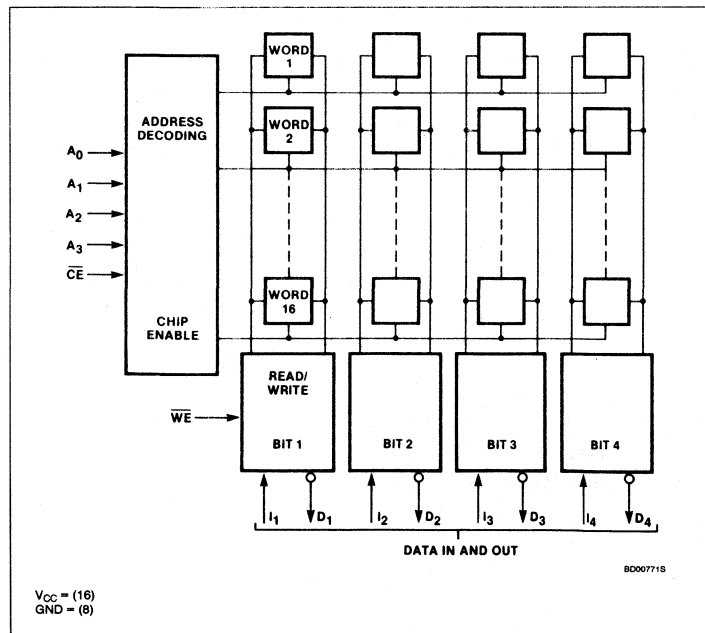
APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

PIN CONFIGURATION



BLOCK DIAGRAM



64-Bit TTL Bipolar RAM (16 × 4)

82S25, 3101A, 74S189

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S25 N • N3101A N • N74S189 N
Plastic Small Outline 300mil wide 16-pin	N82S25 D • N3101A D • N74S189 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V.

PARAMETER	TEST CONDITIONS ⁶	LIMITS			UNIT
		Min	Typ	Max	
Input voltage¹ V _{IL} Low V _{IH} High V _{IC} Clamp ⁷	V _{CC} = 4.75V V _{CC} = 5.25V I _{IN} = -12mA, V _{CC} = 4.75V	2.0		.80 -1.5	V
Output voltage¹ V _{OL} Low ^{2,3} V _{OH} High (74S189)	\overline{CE} = Low I _{OUT} = 16mA, V _{CC} = 4.75V I _{OUT} = -2mA	2.4		0.45	V
Input current⁵ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 10	μA
Output current⁵ I _{OLK} Leakage I _{OS} Short circuit (74S189) I _{OZ} Hi-Z (74S189)	\overline{CE} = High, V _{OUT} = 5.5V, V _{CC} = 4.75V \overline{CE} = Low V _{OUT} = 0V 2.4 ≥ V _{OUT} ≥ 0.4V			100 -100 ± 50	μA mA μA
Supply current⁵ I _{CC} 82S25 3101A 74S189	V _{CC} = 5.25V V _{CC} = 5.25V V _{CC} = 5.25V			105 105 110	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V, \overline{CE} = High		5 8		pF

TRUTH TABLE

MODE	\overline{CE}	\overline{WE}	D _{IN}	82S25	3101A	74S189
				Data Out		
Read	0	1	X	Stored Data	Stored Data	Stored Data
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

64-Bit TTL Bipolar RAM (16 × 4)

82S25, 3101A, 74S189

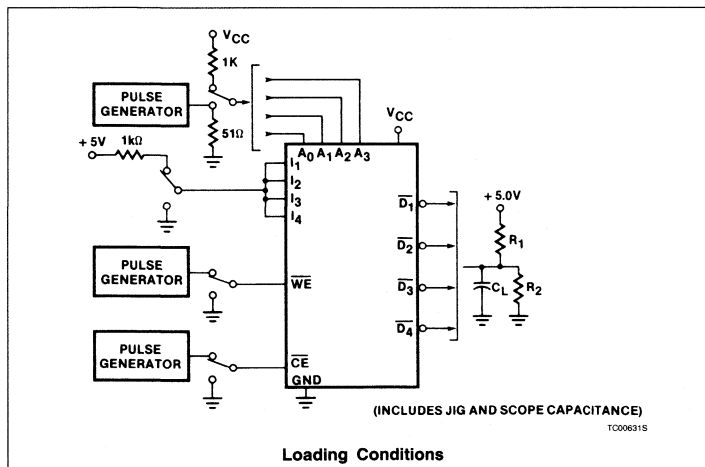
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S25			N3101A, N74S189			UNIT
			Min	Typ	Max	Min	Typ	Max	
Access time									
T_{AA} Address					50			35	ns
T_{CE} Chip enable					35			17	ns
Disable time⁸									
T_{CD}	Output	Chip enable			35			17	ns
Response time⁸									
T_{WD}	Output	Write enable			25			25	ns
Write recovery time									
T_{WR}					50			35	ns
Set-up and hold time									
T_{WSA} Set-up time	Write enable	Address	5			0			ns
T_{WHA} Hold time			5			0			
T_{WSD} Set-up time	Write enable	Data in	30			25			
T_{WHD} Hold time			5			0			
T_{WSC} Set-up time	Write enable	\overline{CE}	0			0			
T_{WHC} Hold time			5			0			
Pulse width⁴									
T_{WP} Write enable			30			25			ns

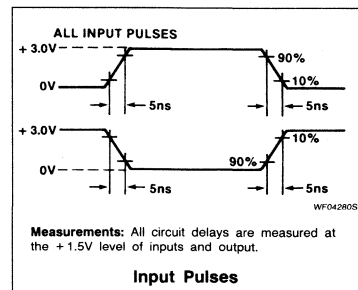
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC} .
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: High = +5.0V, Low = GND.
7. Test each input one at a time.
8. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



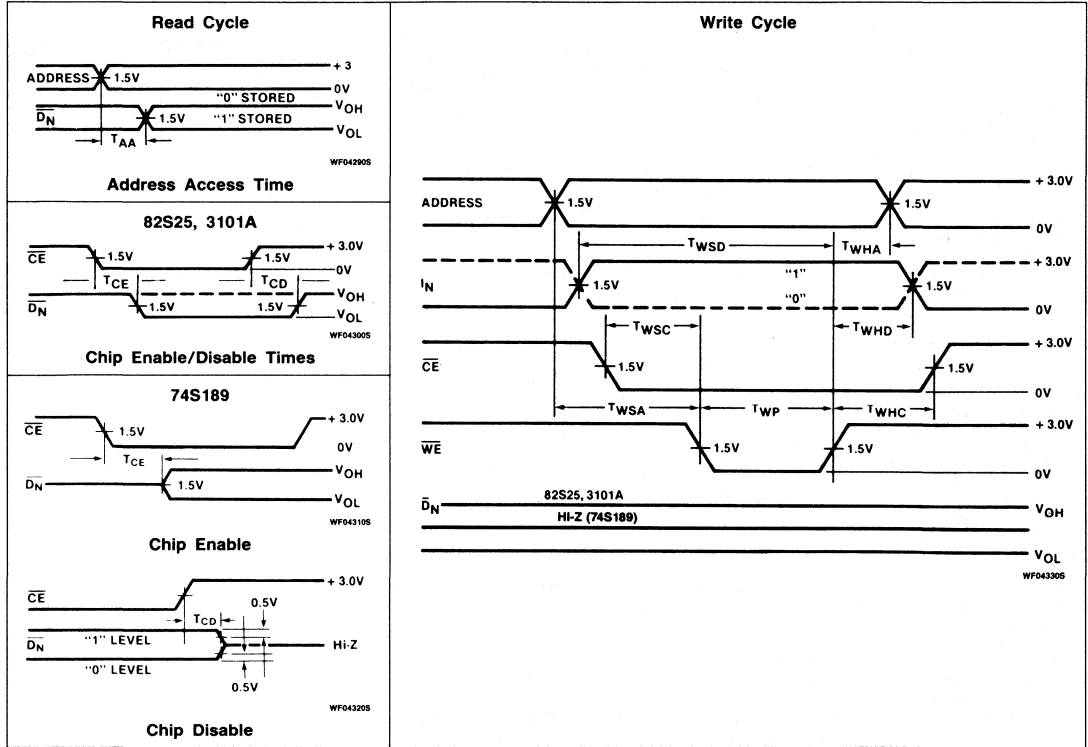
VOLTAGE WAVEFORM



64-Bit TTL Bipolar RAM (16 × 4)

82S25, 3101A, 74S189

TIMING DIAGRAMS



74F189 64-Bit TTL Bipolar RAM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 74F189 is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are Three-state and are in the high-impedance state whenever the Chip Select (\overline{CE}) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Ordering information can be found on the following page.

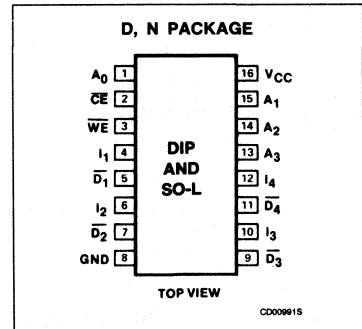
FEATURES

- Address access time: 20ns max
- Power dissipation: 2.9mW/bit typ
- Schottky clamped TTL
- One chip enable input
- I/O
 - Inputs: PNP Buffered
 - Outputs: Three-state

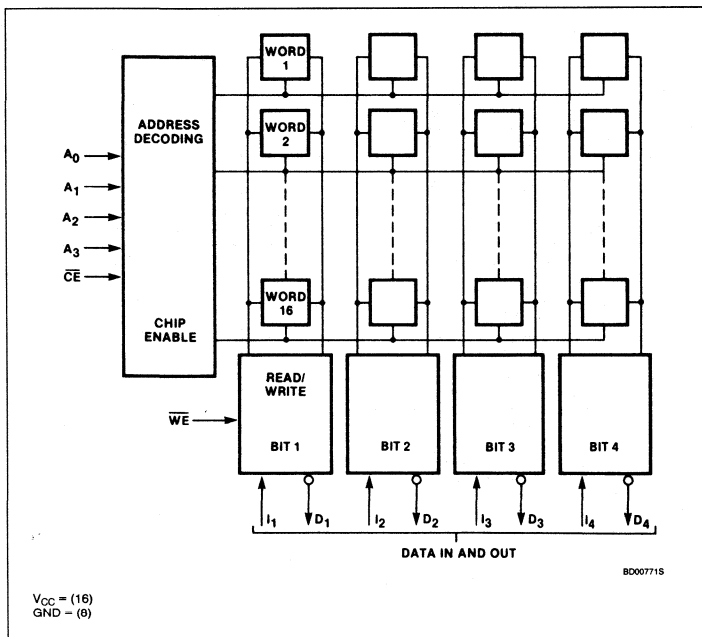
APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

PIN CONFIGURATION



BLOCK DIAGRAM



64-Bit TTL Bipolar RAM (16 × 4)

74F189

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N74F189 N
Plastic Small Outline 300mil wide 16-pin	N74F189 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	-0.5 to +7.0	V _{dc}
V _{IN} Input voltage	-0.5 to +7.0	
V _{OH} Output voltage High	-0.5 to +5.5	
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V.

PARAMETER	TEST CONDITIONS ⁶	LIMITS			UNIT
		Min	Typ	Max	
V _{OH} HIGH-level output voltage	V _{CC} = 4.75V, V _{IH} = 2.0V, V _{IL} = 0.8V, I _{OH} = -3.0mA	2.4			V
V _{OL} LOW-level output voltage	V _{CC} = 4.75V, V _{IH} = 2.0V, V _{IL} = 0.8V, I _{OL} = 20mA		0.35	0.5	
V _{IK} Input clamp voltage	V _{CC} = 5.25V, I _i = -18mA			-1.2	
I _{OZ} Off-state output current, (I _{OZH} , I _{OZL})	V _{CC} = 5.25V, V _{IH} = 2.0V, V _O = 2.4V, 0.5V			± 50	μA
I _{IH} HIGH-level input current	V _{CC} = 5.25V, V _i = 5.5V			40	mA
I _{IL} LOW-level input current	V _{CC} = 5.25V, V _i = 0.5V			-0.6	
I _{OS} Short-circuit output current ₃	V _{CC} = 5.25V	-60		-150	
I _{CC} Supply current (total)	V _{CC} = 5.25V, \overline{WE} , \overline{CS} = GND			100	
Capacitance	V _{CC} = 5.0V				pF
C _{IN} Input	V _{IN} = 2.0V		5		
C _{OUT} Output	V _{OUT} = 2.0V, \overline{CE} = High		8		

TRUTH TABLE

MODE	CE	WE	D _{IN}	DATA OUT
Read	0	1	X	Stored Data
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

X = Don't care

64-Bit TTL Bipolar RAM (16 × 4)

74F189

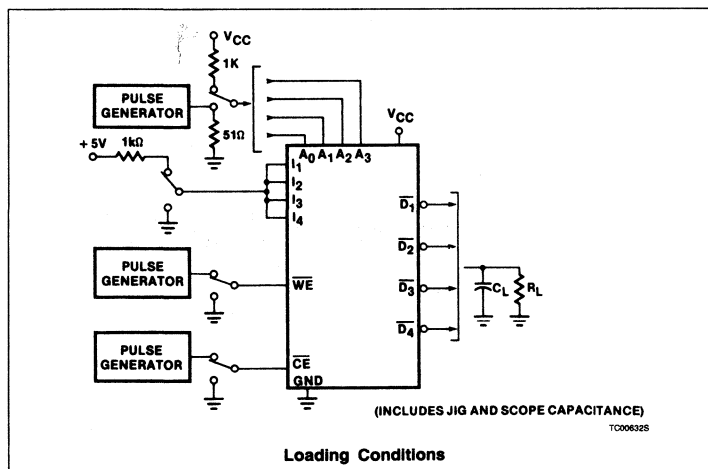
AC ELECTRICAL CHARACTERISTICS $R_L = 500\Omega, C_L = 30pF, 0^\circ C \leq T_A \leq +75^\circ C, 4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time T_{AA} Address T_{CE} Chip enable					20 7.0	ns
Disable time ⁸ T_{CD}	Output	Chip enable			7.0	ns
Response time ⁸ T_{WD}	Output	Write enable			7	ns
Write recovery time T_{WR}	Output	Write enable			7	ns
Set-up and hold time T_{WSA} Set-up time T_{WHA} Hold time	Write enable	Address	3 2			ns
T_{WSD} Set-up time T_{WHD} Hold time	Write enable	Data in	13 2			
T_{WSC} Set-up time T_{WHC} Hold time	Write enable	\overline{CE}	3 2			
Pulse width ⁴ T_{WP} Write enable			15			ns

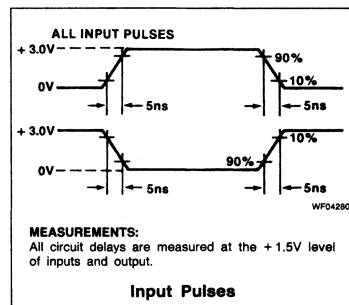
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC} .
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: High = +5.0V, Low = GND.
7. Test each input one at a time.
8. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega, R_2 = 750\Omega$ and $C_L = 5pF$.
9. Subtract 0.2ns from minimum values for SO package.

TEST LOAD CIRCUIT



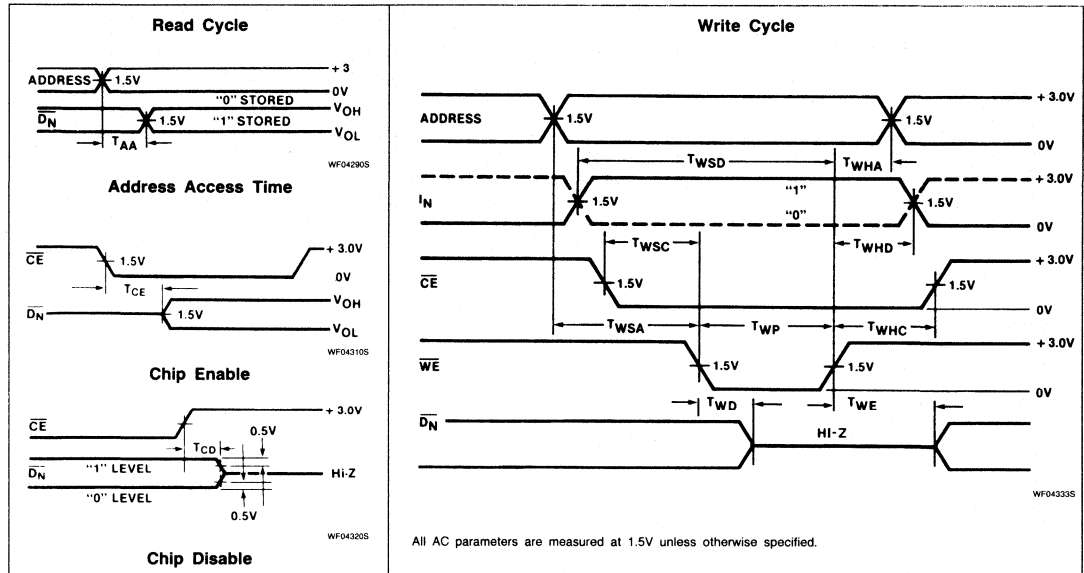
VOLTAGE WAVEFORM



64-Bit TTL Bipolar RAM (16 × 4)

74F189

TIMING DIAGRAMS



256-bit TTL Bipolar RAM

82S16	256-bit RAM (256 x 1)	159
82LS16	256-bit RAM (256 x 1)	163
74S301	256-bit RAM (256 x 1)	167
74LS301	256-bit RAM (256 x 1)	171

82S16 256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S16 is a Read/Write memory array which features 3-state outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

The 82S16 has fast Read access and Write cycle times, and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

The 82S16 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

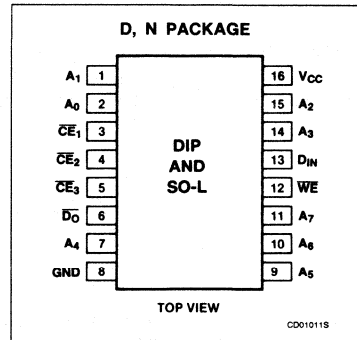
FEATURES

- Address access time: 50ns max
- Write cycle time: 50ns max
- Power dissipation: 1.5mW/bit typ
- Input loading: -100 μ A max
- Output follows complement of data input during Write
- Three chip enable inputs
- On-chip address decoding
- Output: Three-state
- Schottky clamped
- TTL compatible

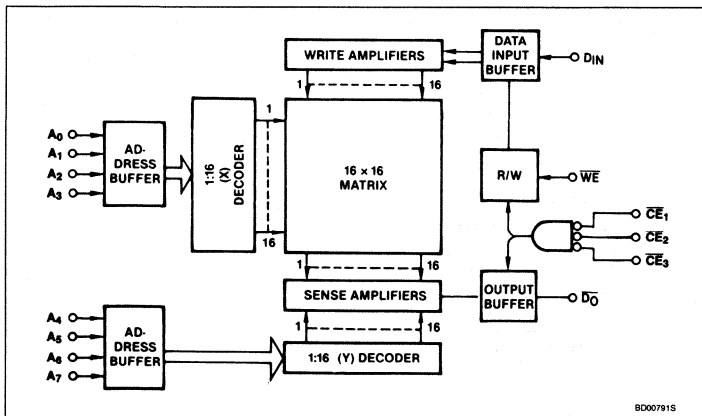
APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 × 1)

82S16

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S16 N
Plastic Small outline 300mil wide 16-pin	N82S16 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OUT} Output voltage High	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ¹	Max	
Input voltage² V _{IH} High V _{IL} Low V _{IC} Clamp ³	V _{CC} = max V _{CC} = min V _{CC} = min, I _{IN} = -12mA	2.0		0.8 -1.5	V
Output voltage² V _{OH} High V _{OL} Low ⁵	V _{CC} = min I _{OH} = -3.2mA I _{OL} = 16mA	2.6	0.35	0.45	V
Input current³ I _{IH} High I _{IL} Low	V _{CC} = max V _{IN} = 5.5V V _{IN} = 0.45V		1 -10	25 -100	μA
Output current I _{oz} Hi-Z State ⁶ I _{os} Short circuit ⁷	V _{OUT} = 5.5V V _{OUT} = 0.45V V _{CC} = max, V _O = 0V		1 -1	40 -40 -70	μA mA
Supply current⁸ I _{CC}	V _{CC} = 5.25V		80	115	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	CE*	WE	D _{IN}	D _{OUT}
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

*"0" = All CE inputs Low; "1" = One or more CE inputs High; X = Don't care.

256-Bit TTL Bipolar RAM (256 × 1)

82S16

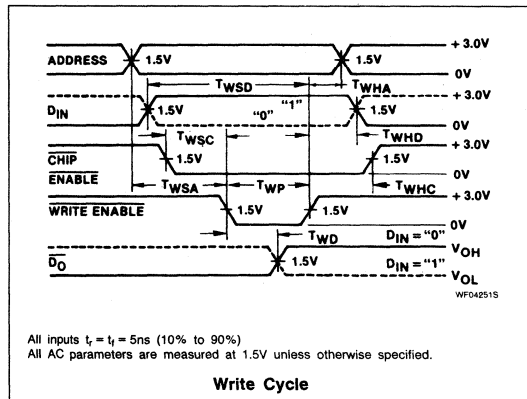
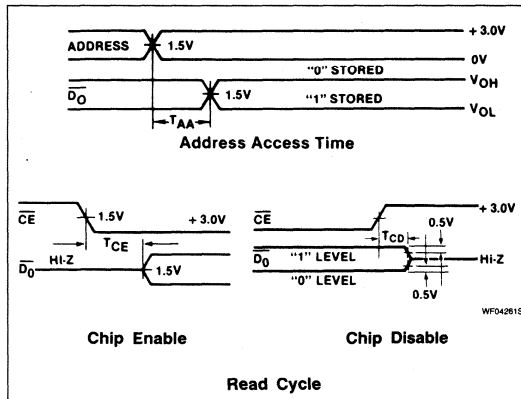
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ¹	Max	
Access time T_{AA} Address T_{CE} Chip enable	Output	Address Chip enable		40 30	50 40	ns
Disable time ¹⁰ T_{CD} T_{WD} Valid time	Output	Chip enable Write enable		30 30	40 40	ns
Set-up and hold time T_{WSA} Set-up time T_{WHA} Hold time	Write enable	Address	15 5	5 0		ns
T_{WSD} Set-up time T_{WHD} Hold time	Write enable	Data in	40 5	30 0		
T_{WSC} Set-up time T_{WHC} Hold time	Write enable	\overline{CE}	10 5	0 0		
Pulse width ⁹ T_{WP} Write enable			30	15		ns

NOTES:

- All typical values are at $V_{CC} = 5\text{V}$, $T_A = +25^\circ\text{C}$.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with a logic low stored and V_{IL} applied to \overline{CE}_1 , \overline{CE}_2 and \overline{CE}_3 .
- Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with V_{IH} applied to \overline{CE}_1 , \overline{CE}_2 and \overline{CE}_3 .
- Duration of the short-circuit should not exceed 1 second.
- t_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.
- Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, and $C_L = 5\text{pF}$.

TIMING DIAGRAMS



All inputs $t_r = t_f = 5\text{ns}$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

256-Bit TTL Bipolar RAM (256 × 1)

82S16

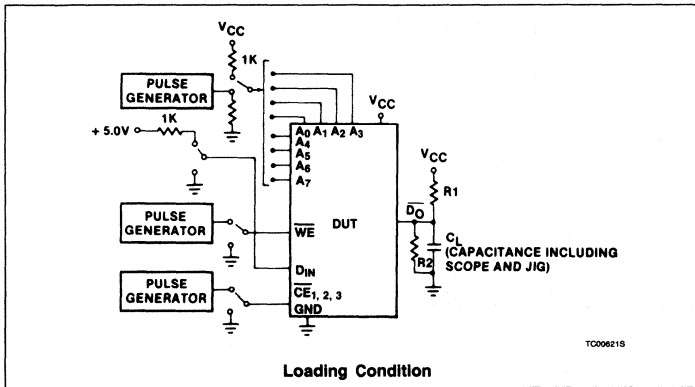
MEMORY TIMING DEFINITIONS

- T_{CE}** Delay between beginning of chip enable low (with address valid) and when data output becomes valid.
- T_{CD}** Delay between when chip enable becomes high and data output is in off state.
- T_{AA}** Delay between beginning of valid address (with chip enable low) and when data output becomes valid.

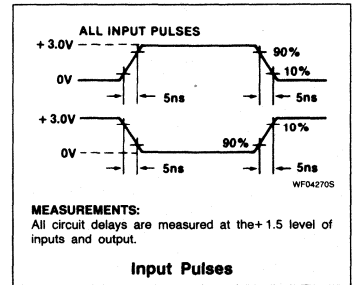
- T_{WSC}** Required delay between beginning of valid chip enable and beginning of Write enable pulse.
- T_{WHD}** Required delay between end of Write enable pulse and of valid input data.
- T_{WP}** Width of Write enable pulse.
- T_{WSA}** Required delay between beginning of valid address and beginning of Write enable pulse.

- T_{WSD}** Required delay between beginning of valid data input and end of Write enable pulse.
- T_{WD}** Delay between beginning of Write enable pulse and when data output reflects complement of data input.
- T_{WHC}** Required delay between end of Write enable pulse and end of chip enable.
- T_{WHA}** Required delay between end of Write enable pulse and end of valid address.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82LS16 256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

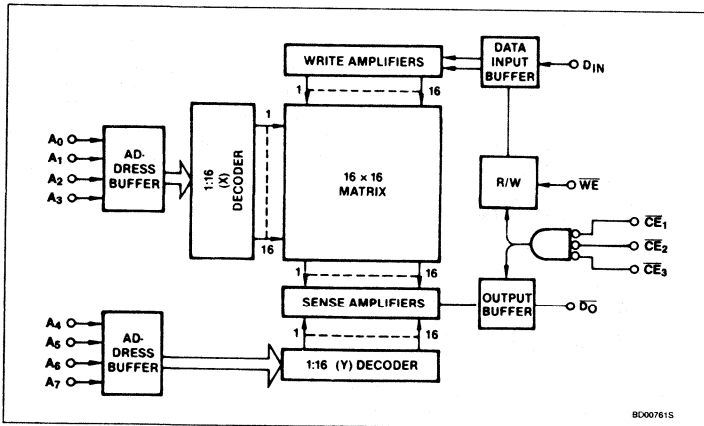
The 82LS16 is a Read/Write memory array which features 3-state outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82LS16 has fast Read access and Write cycle times, as well as low power requirements and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Ordering information can be found on the following page.

BLOCK DIAGRAM



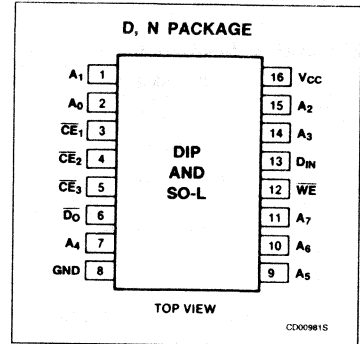
FEATURES

- Address access time: 40ns max
- Write cycle time: 25ns max
- Power dissipation: 0.98mW/bit typ
- Input loading: -100μA max
- Output follows complement of data input during Write
- On-chip address decoding
- Three chip enable inputs
- Output: Three-state
- Schottky clamped
- TTL compatible

APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

PIN CONFIGURATION



256-Bit TTL Bipolar RAM (256 × 1)

82LS16

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82LS16 N
Plastic Small Outline 300mil wide 16-pin	N82LS16 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OUT} Output voltage High (open collector)	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ¹	Max	
Input voltage ² V _{IH} High V _{IL} Low V _{IC} Clamp ³	V _{CC} = 5.25V V _{CC} = 4.75V V _{CC} = 4.75V, I _{IN} = -12mA	2.0		0.8 -1.5	V
Output voltage ² V _{OH} High V _{OL} Low ⁵	V _{CC} = 4.75V I _{OH} = -3.2mA I _{OL} = 16mA	2.6	0.35	0.45	V
Input current ³ I _{IH} High I _{IL} Low	V _{CC} = 5.25V V _{IN} = 5.5V V _{IN} = 0.45V		1 -10	25 -100	μA
Output current I _{OZ} Hi-Z state ⁶ I _{OS} Short circuit ⁷	V _{OUT} = 5.5V V _{OUT} = 0.45V V _{CC} = 5.25V, V _O = 0V		1 -1	40 -40 -70	μA mA
Supply current ⁸ I _{CC}	V _{CC} = 5.25V		50	70	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	\overline{CE}^*	\overline{WE}	D _{IN}	D _{OUT}
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

*"0" = All \overline{CE} inputs Low; "1" = One or more \overline{CE} inputs High. X = Don't care.

256-Bit TTL Bipolar RAM (256 × 1)

82LS16

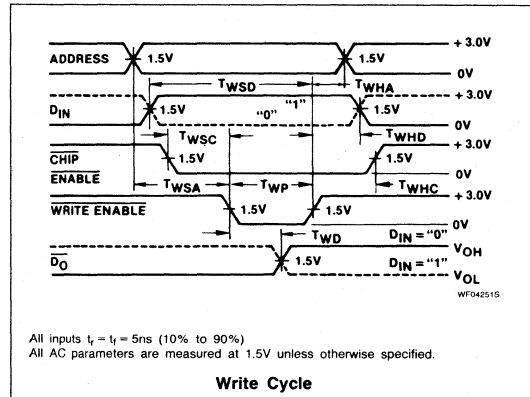
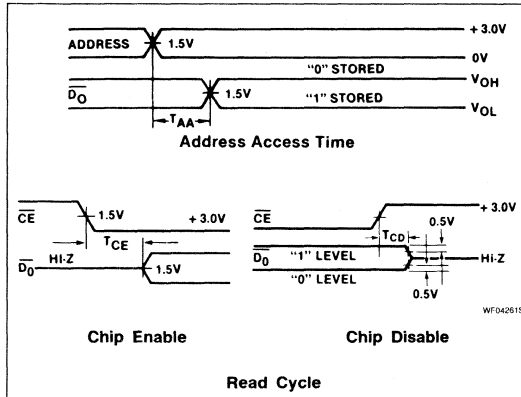
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ¹	Max	
Access time						
T_{AA} Address	Output	Address		30	40	ns
T_{CE} Chip enable	Output	Chip enable		15	25	
Disable time¹⁰						
T_{CD}	Output	Chip enable		15	25	ns
T_{WD} Valid time	Output	Write enable		30	40	
Set-up and hold time						
T_{WSA} Set-up time	Write enable	Address	0	-5		ns
T_{WHA} Hold time			0	-5		
T_{WSD} Set-up time	Write enable	Data in	25	15		
T_{WHD} Hold time			0	-5		
T_{WSC} Set-up time	Write enable	\overline{CE}	0	-5		
T_{WHC} Hold time			0	-5		
Pulse width⁹						
T_{WP} Write enable			25	15		ns

NOTES:

- All typical values are at $V_{CC} = 5V$, $T_A = +25^\circ C$.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with a logic Low stored and V_{IL} applied to \overline{CE}_1 , \overline{CE}_2 and \overline{CE}_3 .
- Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with V_{IH} applied to \overline{CE}_1 , \overline{CE}_2 and \overline{CE}_3 .
- Duration of the short-circuit should not exceed 1 second.
- I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.
- Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$ $R_2 = 750\Omega$ and $C_L = 5pF$.

TIMING DIAGRAMS



All inputs $t_r = t_f = 5ns$ (10% to 90%)
 All AC parameters are measured at 1.5V unless otherwise specified.

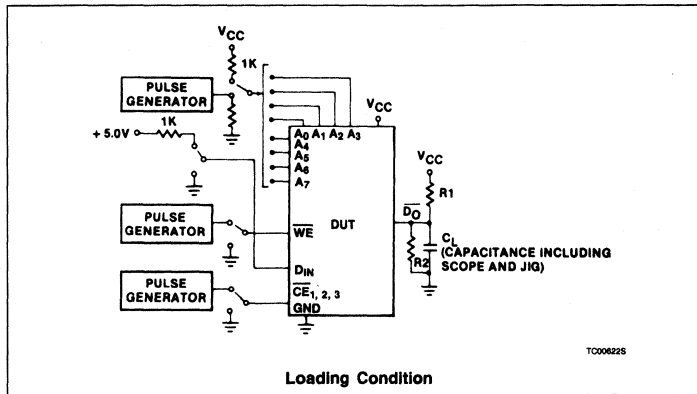
256-Bit TTL Bipolar RAM (256 × 1)

82LS16

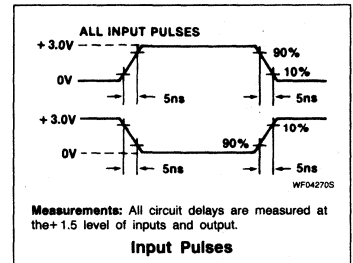
MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of chip enable low (with address valid) and when data output becomes valid.	T_{WSC}	Required delay between beginning of valid chip enable and beginning of Write enable pulse.	T_{WSD}	Required delay between beginning of valid data input and end of Write enable pulse.
T_{CD}	Delay between when chip enable becomes high and data output is in off state.	T_{WHD}	Required delay between end of Write enable pulse and end of valid input data.	T_{WD}	Delay between beginning of Write enable pulse and when data output reflects complement of data input.
T_{AA}	Delay between beginning of valid address (with chip enable low) and when data output becomes valid.	T_{WP}	Width of Write enable pulse.	T_{WHC}	Required delay between end of Write enable pulse and end of chip enable.
		T_{WSA}	Required delay between beginning of valid address and beginning of Write enable pulse.	T_{WHA}	Required delay between end of Write enable pulse and end of valid address.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



74S301 256-Bit TTL RAM

Product Specification

Bipolar Memory Products

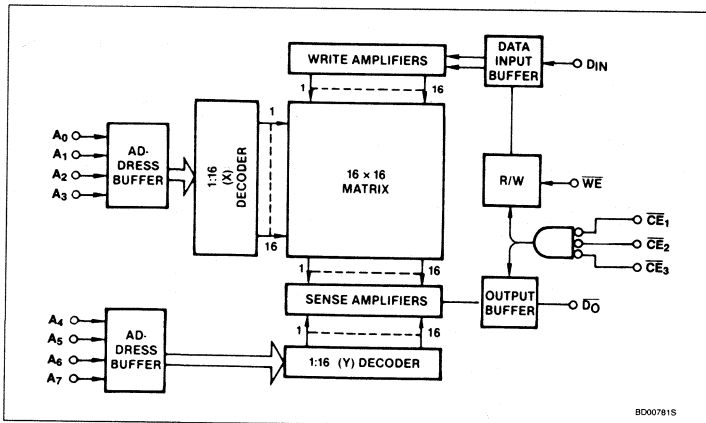
DESCRIPTION

The 74S301 is a Read/Write memory array which features an Open collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write (\overline{D}_O terminal High) permits \overline{D}_O and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

BLOCK DIAGRAM



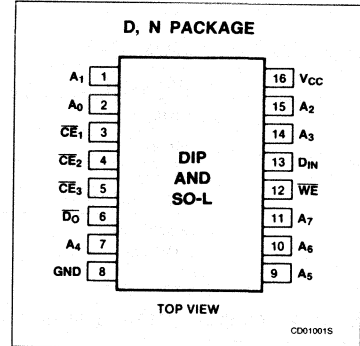
FEATURES

- Address access time: 50ns max
- Write cycle time: 55ns max
- Power dissipation: 1.5mW/bit typ
- Input loading: $-100\mu A$ max
- Output blanking during Write
- On-chip address decoding
- Schottky clamped
- TTL compatible
- Three chip enable inputs
- Output: Open collector

APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

PIN CONFIGURATION



256-Bit TTL Bipolar RAM (256 × 1)

74S301

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N74S301 N
Plastic Small Outline 300mil wide 16-pin	N74S301 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OUT} Output voltage High (open collector)	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ¹	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp ³	V _{CC} = 4.75V V _{CC} = 5.25V V _{CC} = 4.75V, I _{IN} = -12mA	2.0	-1.0	.80 -1.2	V
Output voltage V _{OL} Low ⁵	V _{CC} = 4.75V I _{OL} = 16mA		0.35	0.45	V
Input current I _{IL} Low I _{IH} High	V _{CC} = 5.25V V _{IL} = 0.45V V _{IH} = 2.7V			-100 25	μA
Output current I _{OLK} Leakage	V _{IH} = 2V, V _O = 5.5V			40	μA
Supply current⁶ I _{CC}	V _{CC} = 5.25V, T _A = +125°C		80	130	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	\overline{CE} [*]	WE	D _{IN}	D _{OUT}
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

*"0" = All \overline{CE} inputs Low; "1" = One or more \overline{CE} inputs High.
X = Don't care.

256-Bit TTL Bipolar RAM (256 × 1)

74S301

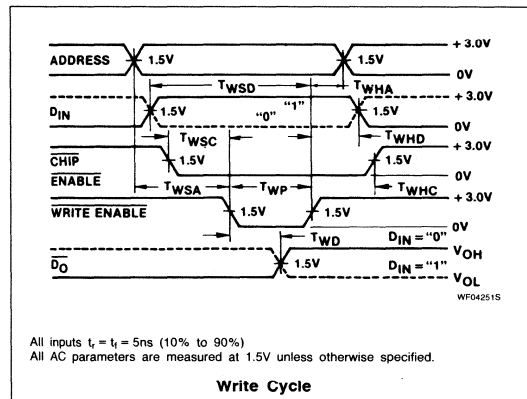
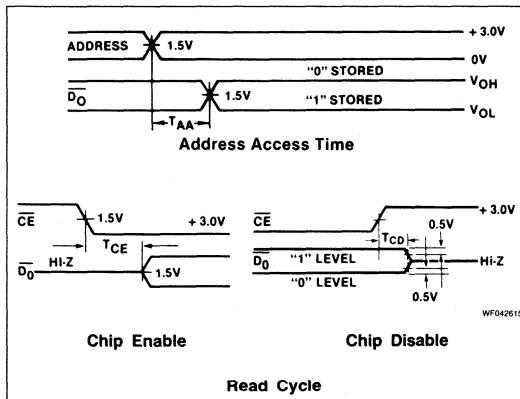
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega, R_2 = 600\Omega, C_L = 30pF, 0^\circ C \leq T_A \leq +75^\circ C, 4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ¹	Max	
Access time						
T_{AA} Address	Output	Address		40	50	ns
T_{CE} Chip enable	Output	Chip enable		30	40	
Disable time¹⁰						
T_{CD}	Output	Chip enable		30	40	ns
T_{WD} Valid time	Output	Write enable		30	40	
Set-up and hold time						
T_{WSA} Set-up time	Write enable	Address	20	5		ns
T_{WHA} Hold time	Write enable	Address	5	0		
T_{WSD} Set-up time	Write enable	Data in	40	30		
T_{WHD} Hold time	Write enable	Data in	5	0		
T_{WSC} Set-up time	Write enable	\overline{CE}	10	0		
T_{WHC} Hold time	Write enable	\overline{CE}	5	0		
Pulse width⁹						
T_{WP} Write enables			30	15		ns

NOTES:

1. All typical values are at $V_{CC} = 5V, T_A = +25^\circ C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1, \overline{CE}_2$ and \overline{CE}_3 .
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC} .
6. Measured with V_{IH} applied to $\overline{CE}_1, \overline{CE}_2$ and \overline{CE}_3 .
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega, R_2 = 750\Omega$ and $C_L = 5pF$.

TIMING DIAGRAMS



All inputs $t_r = t_f = 5ns$ (10% to 90%)
 All AC parameters are measured at 1.5V unless otherwise specified.

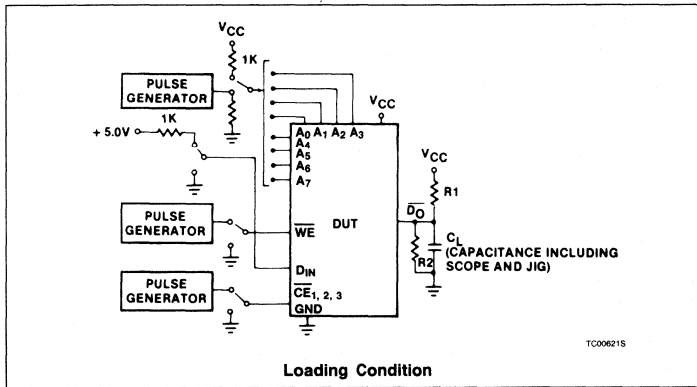
256-Bit TTL Bipolar RAM (256 × 1)

74S301

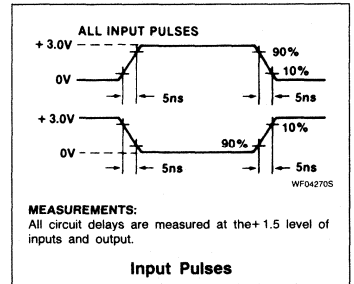
MEMORY TIMING DEFINITIONS

<p>T_{CE} Delay between beginning of chip enable low (with address valid) and when data output becomes valid.</p> <p>T_{CD} Delay between when chip enable becomes high and data output is in off state.</p> <p>T_{AA} Delay between beginning of valid address (with chip enable low) and when data output becomes valid.</p>	<p>T_{WSC} Required delay between beginning of valid chip enable and beginning of Write enable pulse.</p> <p>T_{WHD} Required delay between end of Write enable pulse and end of valid input data.</p> <p>T_{WTP} Width of Write enable pulse.</p> <p>T_{WSA} Required delay between beginning of valid address and beginning of Write enable pulse.</p>	<p>T_{WSD} Required delay between beginning of valid data input and end of Write enable pulse.</p> <p>T_{WD} Delay between beginning of Write enable pulse and when data output reflects complement of data input.</p> <p>T_{WHC} Required delay between end of Write enable pulse and end of chip enable.</p> <p>T_{WHA} Required delay between end of Write enable pulse and end of valid address.</p>
-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



74LS301 256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 74LS301 is a Read/Write memory array which features an Open collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write (\overline{D}_O terminal High) permits \overline{D}_O and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

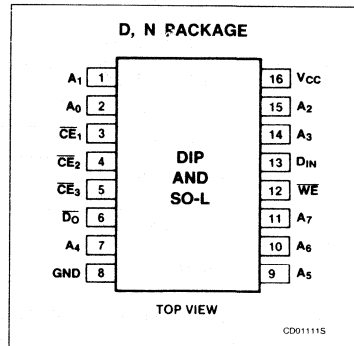
FEATURES

- Address access time: 40ns max
- Write cycle time: 25ns max
- Power dissipation: 0.98mW/bit typ
- Input loading: $-100\mu A$ max
- Output blanking during Write
- On-chip address decoding
- Schottky clamped
- TTL compatible
- Three chip enable inputs
- Open collector output

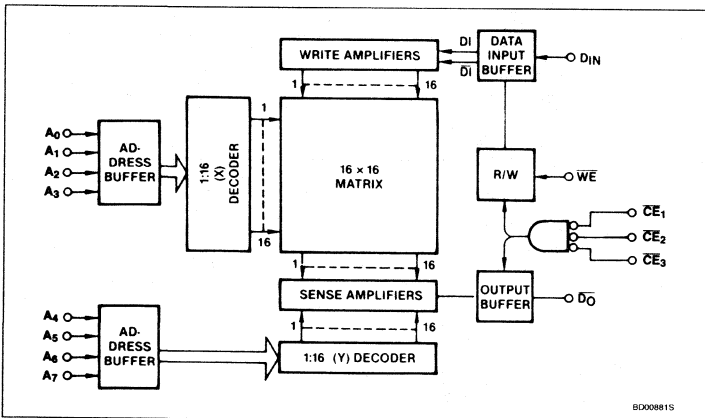
APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 × 1)

74LS301

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N74LS301 N
Plastic Small Outline 300mil wide 16-pin	N74LS301 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OUT} Output voltage High (open collector)	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage ² V _{IL} Low V _{IH} High V _{IC} Clamp ³	V _{CC} = 4.75V V _{CC} = 5.25V V _{CC} = 4.75V, I _{IN} = -12mA	2.0		.8 -1.2	V
Output voltage V _{OL} Low ⁵	V _{CC} = 4.75V I _{OL} = 16mA			0.45	V
Input current ² I _{IL} Low I _{IH} High	V _{CC} = 5.25V V _{IL} = 0.45V V _{IH} = 2.7V			-100 25	μA
Output current I _{OLK} Leakage ⁵	V _{IH} = 2V, V _O = 5.5V			40	μA
Supply current ⁸ I _{CC}	V _{CC} = 5.25V		50	70	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	\overline{CE}^*	\overline{WE}	D _{IN}	D _{OUT}
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

**"0" = All \overline{CE} inputs Low; "1" = One or more \overline{CE} inputs High.
X = Don't care.

256-Bit TTL Bipolar RAM (256 × 1)

74LS301

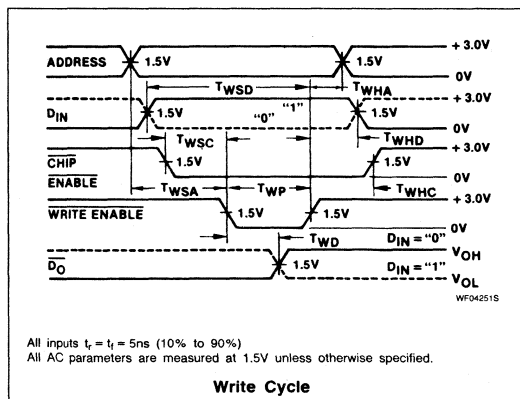
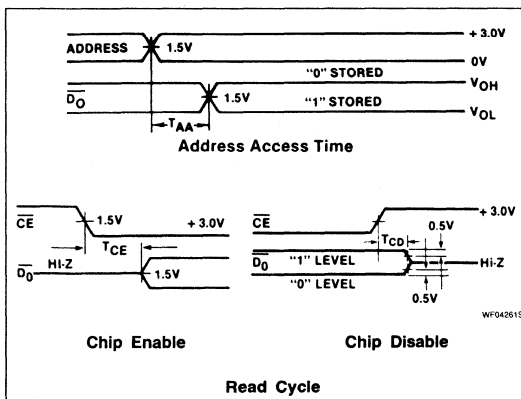
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega, R_2 = 600\Omega, C_L = 30\text{pF}, 0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}, 4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ¹	Max	
Access time						
T_{AA} Address	Output	Address		30	40	ns
T_{CE} Chip enable	Output	Chip enable		15	25	
Disable time¹⁰						
T_{CD}	Output	Chip enable		15	25	ns
T_{WD} Valid time	Output	Write enable		30	40	
Set-up and hold time						
T_{WSA} Set-up time	Write enable	Address	0	-5		
T_{WHA} Hold time			0	-5		
T_{WSD} Set-up time	Write enable	Data in	25	15		ns
T_{WHD} Hold time			0	-5		
T_{WSC} Set-up time	Write enable	\overline{CE}	0	-5		
T_{WHC} Hold time			0	-5		
Pulse width⁹						
T_{WP} Write enable			25	15		ns

NOTES:

1. All typical values are at $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1, \overline{CE}_2$ and \overline{CE}_3 .
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC} .
6. Measured with V_{IH} applied to $\overline{CE}_1, \overline{CE}_2$ and \overline{CE}_3 .
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from logic levels with $R_1 = 750\Omega, R_2 = 750\Omega$ and $C_L = \text{pF}$

TIMING DIAGRAMS



All inputs $t_r = t_f = 5\text{ns}$ (10% to 90%)
 All AC parameters are measured at 1.5V unless otherwise specified.

256-Bit TTL Bipolar RAM (256 × 1)

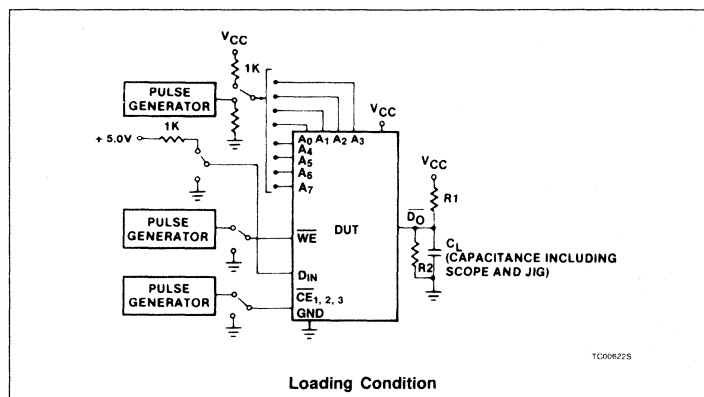
74LS301

MEMORY TIMING DEFINITIONS

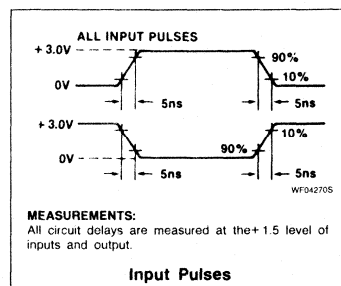
T_{CE}	Delay between beginning of chip enable low (with address valid) and when data output becomes valid.	T_{WSC}	Required delay between beginning of valid chip enable and beginning of Write enable pulse.
T_{CD}	Delay between when chip enable becomes high and data output is in off state.	T_{WHD}	Required delay between end of Write enable pulse and end of valid input data.
T_{AA}	Delay between beginning of valid address (with chip enable low) and when data output becomes valid.	T_{WP}	Width of Write enable pulse.
		T_{WSA}	Required delay between beginning of valid address and beginning of Write enable pulse.

T_{WSD}	Required delay between beginning of valid data input and end of Write enable pulse.
T_{WD}	Delay between beginning of Write enable pulse and when data output reflects complement of data input.
T_{WHC}	Required delay between end of Write enable pulse and end of chip enable.
T_{WHA}	Required delay between end of Write enable pulse and end of valid address.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5 level of inputs and output.

Byte-Organized RAM

82S09/82S09A	576-bit Bipolar RAM (64 x 9).....	177
82S19	576-bit Bipolar RAM (64 x 9).....	181
82S212/82S212A	2304-bit Bipolar RAM (256 x 9).....	185
8X350	2048-bit Bipolar RAM (256 x 8).....	189

82S09 82S09A 576-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth. The 82S09/09A features Open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

Ordering information can be found on the following page.

The 82S09 and 82S09A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

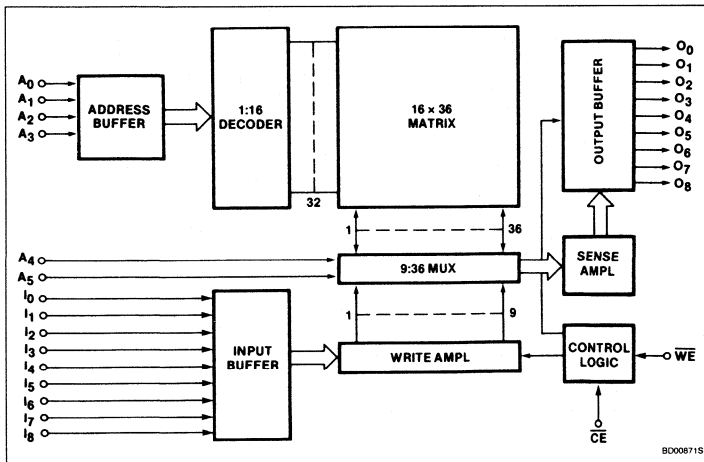
FEATURES

- Address access time:
 - N82S09: 45ns max
 - N82S09A: 35ns max
- Write cycle time:
 - N82S09/09A: 45ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- Output is Non-Blanked during Write
- One chip enable input
- Outputs: Open collector

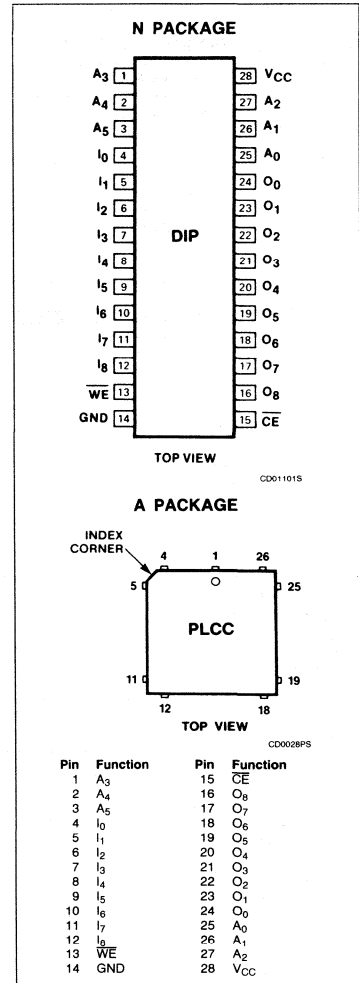
APPLICATIONS

- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

BLOCK DIAGRAM



PIN CONFIGURATION



576-Bit TTL Bipolar RAM (64 × 9)

82S09, 82S09A

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 600mil wide 28-pin	N82S09 N • N82S09A N
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82S09 A • N82S09A A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage ¹ V _{IL} Low V _{IH} High V _{IC} Clamp ²	V _{CC} = 4.75V V _{CC} = 5.25V V _{CC} = 4.75V min, I _{IN} = -12mA	2.0		0.8 -1.5	V
Output voltage ¹ V _{OL} Low ³	V _{CC} = 4.75V, I _{OL} = 8.0mA			0.5	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 25	μA
Output current I _{OLK} Leakage ⁴	V _{CC} = 5.25V, V _{OUT} = 5.5V			40	μA
Supply current ⁵ I _{CC}	V _{CC} = 5.25V			190	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

Refer to notes on next page.

TRUTH TABLE

MODE	\overline{CE}	\overline{WE}	I _N	O _N
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

X = Don't care

576-Bit TTL Bipolar RAM (64 × 9)

82S09, 82S09A

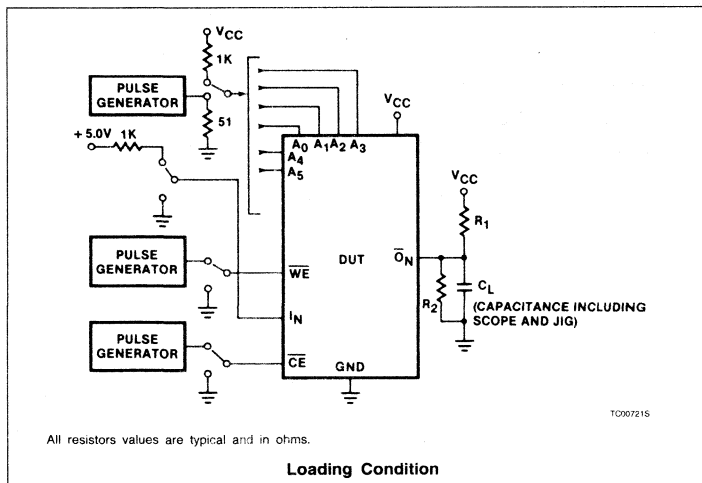
AC ELECTRICAL CHARACTERISTICS $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S09			N82S09A			UNIT
			Min	Typ	Max	Min	Typ	Max	
Access time									
T_{AA} Address					45			35	ns
T_{CE} Chip enable					30			25	
Disable time^B									
T_{CD}	Output	Chip enable			30			25	ns
T_{WA} Valid time	Output	Write enable			30			25	
Set-up and hold time									
T_{WSA} Set-up time	Write enable	Address	5			5			ns
T_{WHA} Hold time	Write enable	Address	5			5			
T_{WSD} Set-up time	Write enable	Data in	35			30			
T_{WHD} Hold time	Write enable	Data in	5			5			
T_{WSC} Set-up time	Write enable	\overline{CE}	5			5			
T_{WHC} Hold time	Write enable	\overline{CE}	5			5			
Pulse width^B									
T_{WP} Write enable			35			35			ns

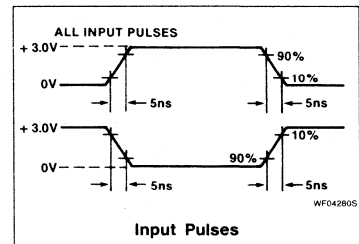
NOTES:

1. All voltage values are with respect to network ground.
2. Test each input one at a time.
3. Measured with the logic low stored. Output sink current is applied through a resistor to V_{CC} .
4. Measured with V_{IH} applied to \overline{CE} .
5. I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
8. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



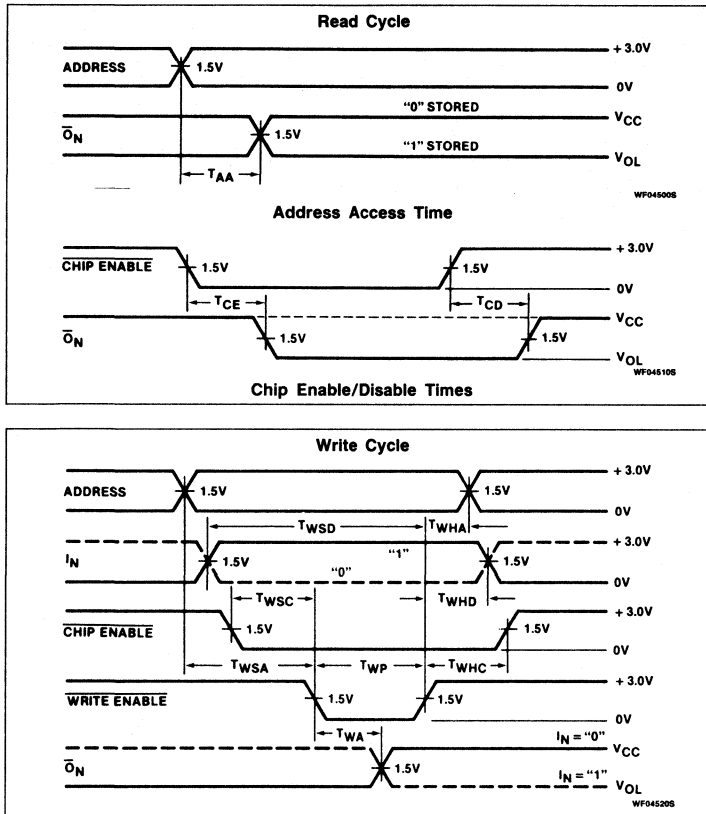
VOLTAGE WAVEFORM



576-Bit TTL Bipolar RAM (64 × 9)

82S09, 82S09A

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

- T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
- T_{AA} Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
- T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
- T_{WHD} Required delay between end of Write Enable pulse and end of valid input Data.
- T_{WP} Width of Write Enable pulse.
- T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.
- T_{WSD} Required delay between beginning of valid Data input and end of Write Enable pulse.
- T_{WD} Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
- T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.
- T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.
- T_{WR} Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)
- T_{WA} Delay between beginning of Write Enable pulse and when data output reflects complement of data input.

82S19 576-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S19 features Open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

Ordering information can be found on the following page.

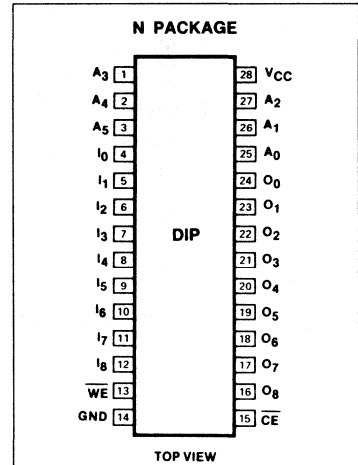
FEATURES

- Address access time: 35ns max
- Write cycle time: 45ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: -100µA max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- One chip enable input
- Output is blanked during write
- Outputs: Open collector

APPLICATIONS

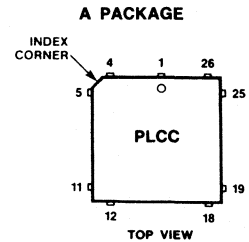
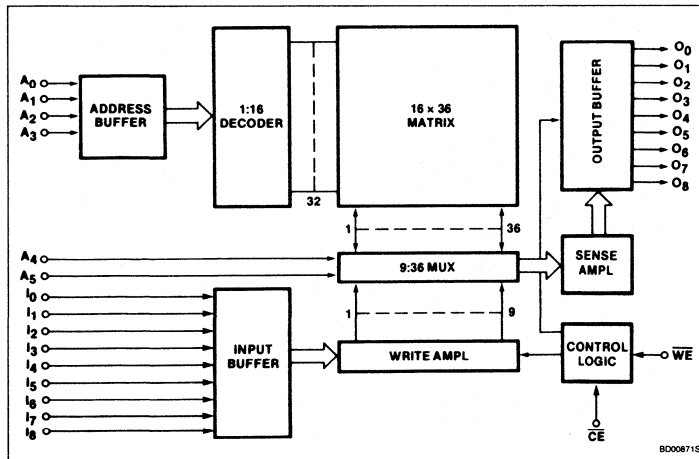
- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

PIN CONFIGURATION



CD00101S

BLOCK DIAGRAM



CD0028PS

Pin	Function	Pin	Function
1	A ₃	15	CE
2	A ₄	16	O ₈
3	A ₅	17	O ₇
4	I ₀	18	O ₆
5	I ₁	19	O ₅
6	I ₂	20	O ₄
7	I ₃	21	O ₃
8	I ₄	22	O ₂
9	I ₅	23	O ₁
10	I ₆	24	O ₀
11	I ₇	25	A ₀
12	I ₈	26	A ₁
13	WE	27	A ₂
14	GND	28	V _{CC}

576-Bit TTL Bipolar RAM (64 × 9)

82S19

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 600mil wide 28-pin	N82S19 N
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82S19 A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp ²	V _{CC} = 4.75V V _{CC} = 5.25V V _{CC} = 4.75V, I _{IN} = -12mA	2.0		0.8 -1.5	V
Output voltage V _{OL} Low ³	V _{CC} = 4.75V, I _{OL} = 8.0mA			0.5	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 26	μA
Output current I _{OLK} Leakage ⁴	V _{CC} = 5.25V, V _{OUT} = 5.5V			40	μA
Supply current ^{3,5} I _{CC}	V _{CC} = 5.25V			190	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

Refer to notes on next pages.

TRUTH TABLE

MODE	CE	WE	I _N	O _N
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care

576-Bit TTL Bipolar RAM (64 × 9)

82S19

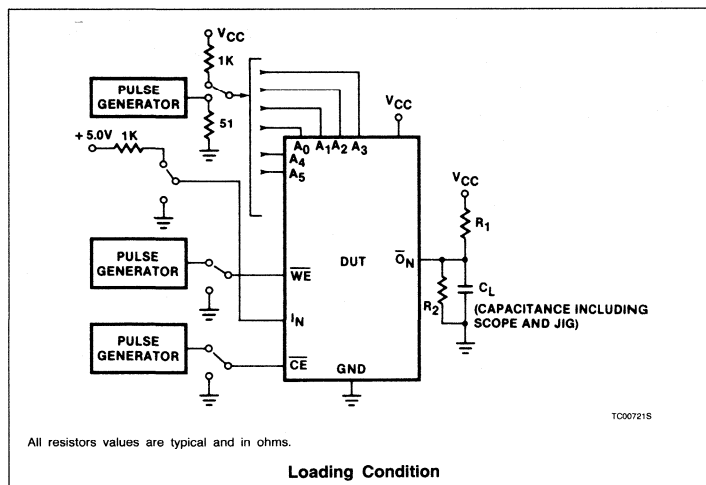
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega, R_2 = 600\Omega, C_L = 30\text{pF}, 0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}, 4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						
T_{AA} Address					35	ns
T_{CE} Chip enable					25	
T_{CD} Disable time	Output	Chip enable			25	ns
T_{WD} Valid time	Output	Write enable			25	
T_{WR} Write recovery time	Output	Write enable			25	
Set-up and hold time						
T_{WSA} Set-up time	Write enable	Address	5			ns
T_{WHA} Hold time			5			
T_{WSD} Set-up time	Write enable	Data in	30			
T_{WHD} Hold time			5			
T_{WSC} Set-up time	Write enable	\overline{CE}	5			
T_{WHC} Hold time			5			
Pulse width⁶						
T_{WP} Write enable			35			ns

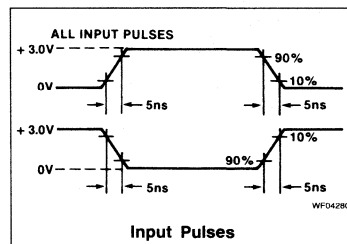
NOTES:

1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1, \overline{CE}_2$ and \overline{CE}_3 .
4. Measured with V_{IH} applied to \overline{CE} .
5. I_{CC} is measured with the write enable and chip enable inputs grounded, all other inputs at 4.5V and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT



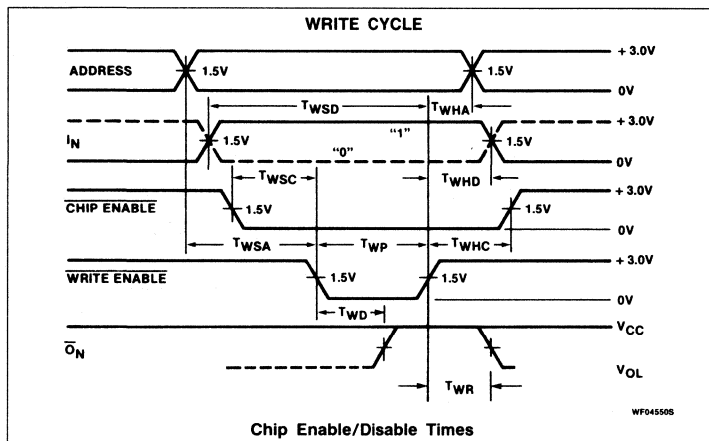
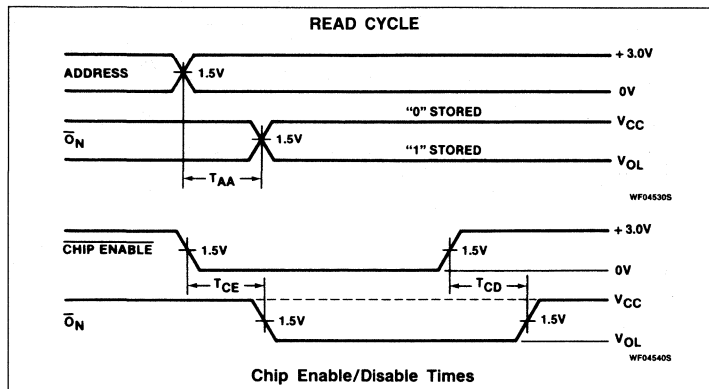
VOLTAGE WAVEFORM



576-Bit TTL Bipolar RAM (64 × 9)

82S19

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

- T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
- T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state.
- T_{AA} Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
- T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
- T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.
- T_{WP} Width of Write Enable pulse.
- T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.
- T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.
- T_{WD} Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
- T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.
- T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.
- T_{WR} Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)

82S212 82S212A 2304-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of the 82S212 and 82S212A allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 and 82S212A are ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

Data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of Read/Write operations using a common bus.

Ordering information can be found on the following page.

The 82S212 and 82S212A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

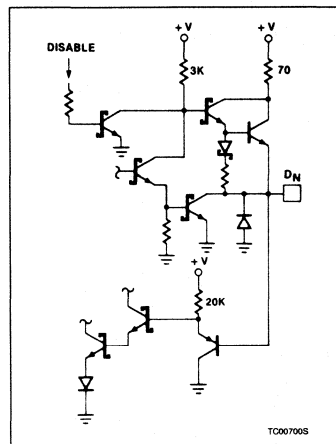
- Address access time:
 - 82S212: 45ns max
 - 82S212A: 35ns max
- Power dissipation: 0.3mW/bit typ
- Schottky clamped TTL

- One chip enable input
- Common I/O
 - Inputs: PNP Buffered
 - Outputs: Three-state

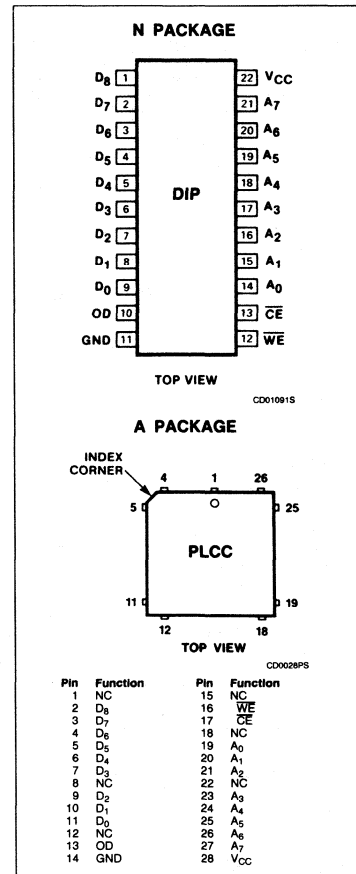
APPLICATIONS

- Cache memory
- Buffer storage
- Writable control store

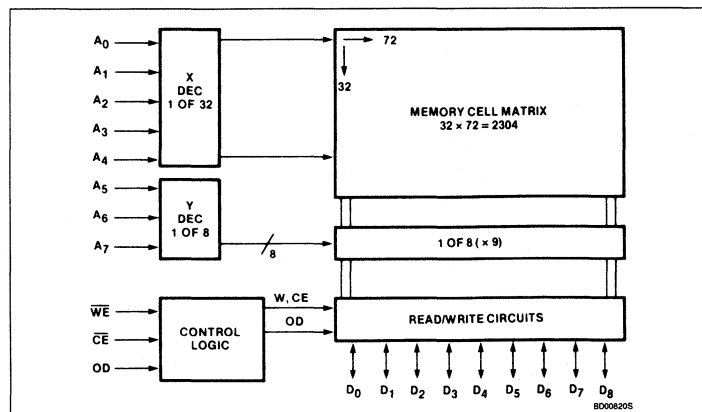
TYPICAL I/O STRUCTURE



PIN CONFIGURATION



BLOCK DIAGRAM



2304-Bit TTL Bipolar RAM (256 × 9)

82S212, 82S212A

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 400 mil wide 22-pin	N82S212 N • N82S212A N
Plastic Leaded Chip Carrier 450 mil sq 28-pin	N82S212 A • N82S212A A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Off-state output voltage	+5.5	V _{dc}
T _A Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ³	Max	
Input voltage ² V _{IL} Low V _{IH} High V _{IC} Clamp ⁴	V _{CC} = 4.75V V _{CC} = 5.25V V _{CC} = 4.75V, I _{IN} = -12mA	2.0		0.80 -1.5	V
Output voltage ² V _{OH} High V _{OL} Low	I _{OH} = -2mA V _{CC} = 4.75V, I _{OL} = 8.0mA	2.4		0.5	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 25	μA
Output current I _{oz} Hi-Z State I _{os} Short circuit ^{4,5}	\overline{CE} = High, or OD = High, V _{OUT} = 5.5V \overline{CE} = High or OD = High, V _{OUT} = 0.5V \overline{CE} = OD = Low, V _{OUT} = 0V	-15		40 -100 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		135	185	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	\overline{WE}	\overline{CE}	OD	D _N IN/OUT
Disable output	X	X	1	High Z
Disable R/W	X	1	X	High Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

2304-Bit TTL Bipolar RAM (256 × 9)

82S212, 82S212A

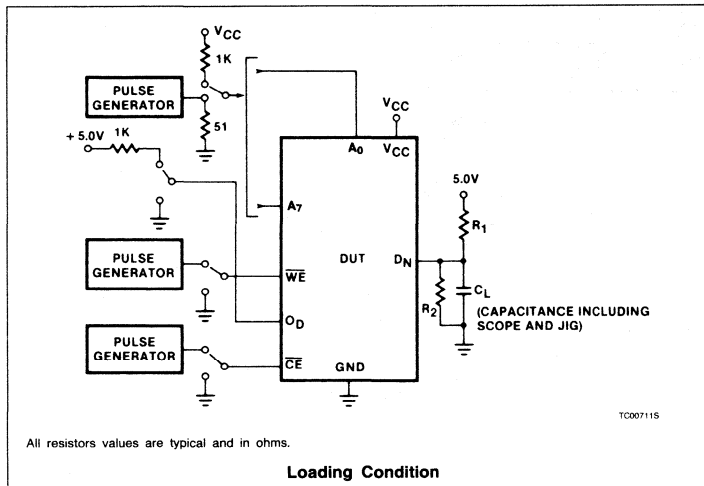
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER ¹	TO	FROM	N82S212			N82S212A			UNIT
			Min	Typ ³	Max	Min	Typ ³	Max	
Access time T_{AA} Address	Output	Address			45			35	ns
Enable time T_{OE} Output T_{CE} Output	Output Output	OD Chip enable	5		25 25			25 25	ns
Disable time⁶ T_{OD} Output T_{CD} Output	Output Output	OD Chip enable			25 25			25 25	ns
Pulse width T_{WP} Write			25			25			ns
Set-up and hold time T_{SWC} Set-up time T_{WHD} Hold time	Write Chip enable	Chip enable Write	5 5			5 5			ns
T_{WSD} Set-up time T_{WHD} Hold time	Write Data	Data Write	25 5			25 5			
T_{WSA} Set-up time T_{WHA} Hold time	Write Address	Address Write	5 5			5 5			
T_{SO} Set-up time (from disabled state) T_{HO} Hold time	Chip enable OD	OD Chip enable	5 5			5 5			

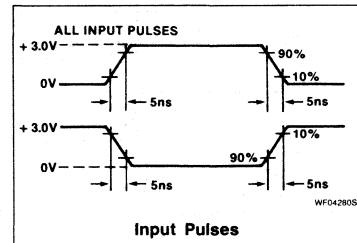
NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



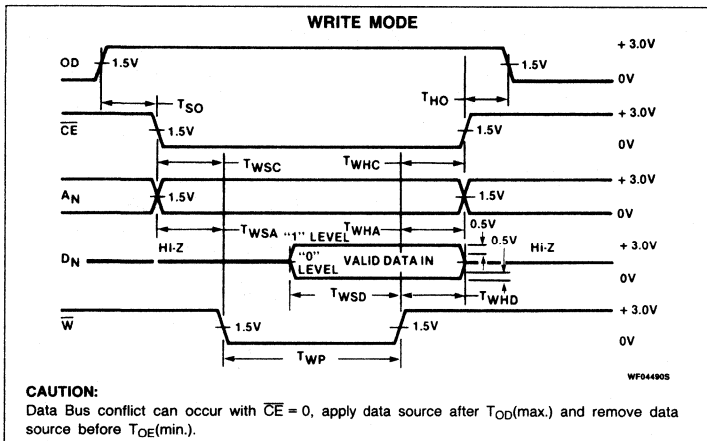
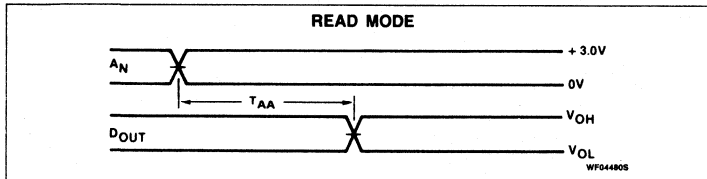
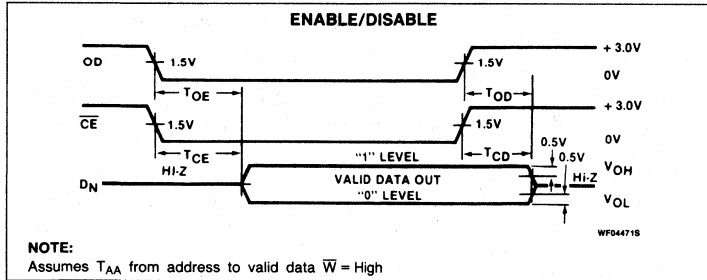
VOLTAGE WAVEFORM



2304-Bit TTL Bipolar RAM (256 × 9)

82S212, 82S212A

TIMING DIAGRAMS



8X350 2K-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X305 based system. Internal circuitry is provided for direct use in 8X305 applications. When used with the 8X305, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with three-state outputs.

Ordering information can be found on the following page.

The 8X350 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

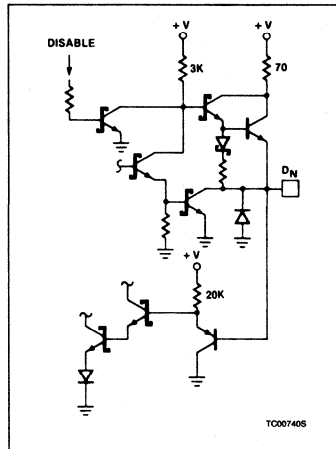
- On-chip address latches
- Schottky clamped
- One master enable input
- Directly interfaces with the 8X305 bipolar microprocessor with no external logic

- May be used on left or right bank
- Common I/O:
 - Inputs: PNP buffered
 - Outputs: Three-state

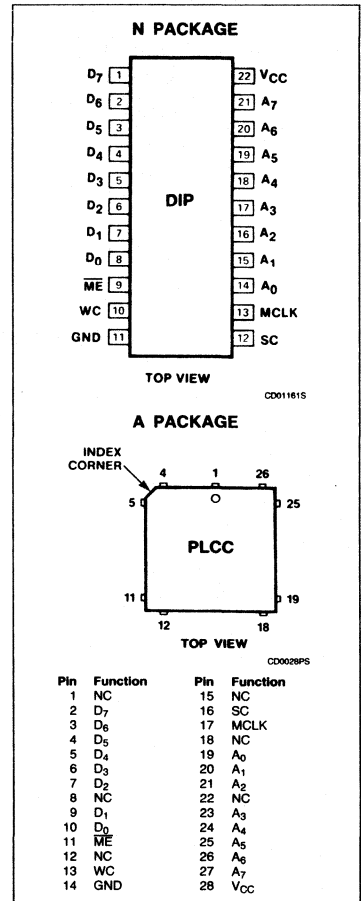
APPLICATIONS

- 8X300 or 8X305 working storage

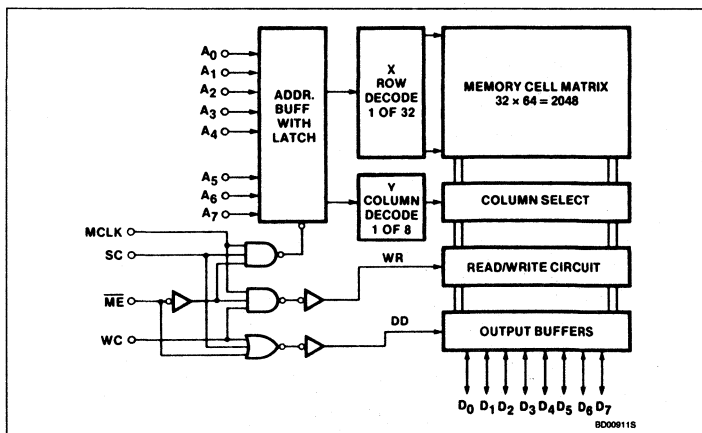
TYPICAL I/O STRUCTURE



PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar RAM (256 × 8)

8X350

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 400mil wide 22-pin	N8X350 N
Plastic Leaded Chip Carrier 450mil sq 28-pin	N8X350 A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High	+5.5	V _{dc}
V _O Off-state	+5.5	
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp ³	V _{CC} = 4.75V V _{CC} = 5.25V V _{CC} = 4.75V, I _{IN} = -12mA	2.0		0.8 -1.2	V
Output voltage V _{OL} Low ⁴ V _{OH} High ⁵	V _{CC} = 4.75V I _{OL} = 9.6mA I _{OH} = -2mA	2.4		0.5	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 25	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ^{3,6}	\overline{ME} = High, V _{OUT} = 5.5V \overline{ME} = High, V _{OUT} = 0.5V SC = WC, \overline{ME} = Low, V _{OUT} = 0V, Stored High	-15		40 -100 -70	μA mA
Supply current ⁷ I _{CC}	V _{CC} = 5.25V			185	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{ME} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

2K-Bit TTL Bipolar RAM (256 × 8)

8X350

TRUTH TABLE

MODE	\overline{ME}	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address Disable data out	1	X	X	X	High Z data out
Input new address	0	1	0	1	Address High Z
Hold address Disable data out	0	1	0	0	High Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	High Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state ¹²	0	1	1	1	-
Hold address ¹² Disable data out	0	1	1	0	High Z data out

NOTE:

X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Enable time T_{E1} Output T_{E2} Output	Data out Data out	SC- ME-			35 35	ns
Disable time ¹³ T_{D1} Output T_{D2} Output	Data out Data out	SC+ ME+			35 35	ns
Pulse width ⁸ T_W Master clock			40			ns
Set-up and hold time T_{SA} Set-up time T_{HA} Hold time	MCLK- Address	Address MCLK-	30 5			ns
T_{SD} Set-up time T_{HD} Hold time	MCLK- Data in	Data in MCLK-	35 5			
T_{S3} Set-up time T_{H3} Hold time	MCLK- ME+	\overline{ME} - MCLK-	40 5			
T_{S1} Set-up time T_{H2} Hold time	MCLK- ME-	\overline{ME} - MCLK-	30 5			
T_{S2} Set-up time T_{H1} Hold time	ME- SC-	SC-, WC- MCLK-	0 5			
T_{H4} Hold time	WC- MCLK-	MCLK-	5 5			

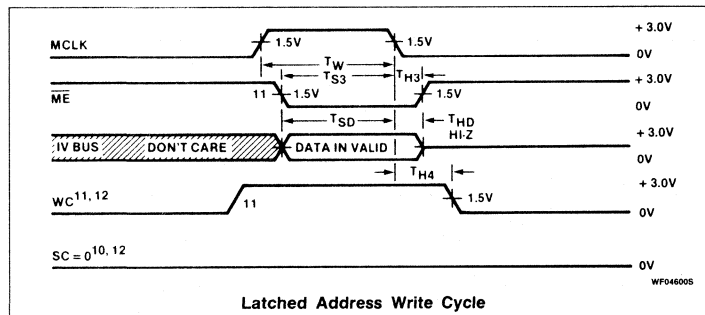
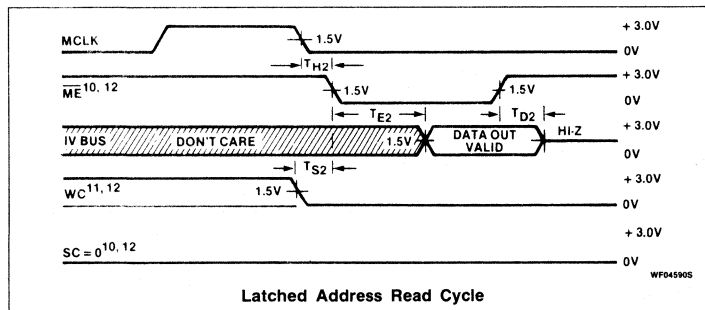
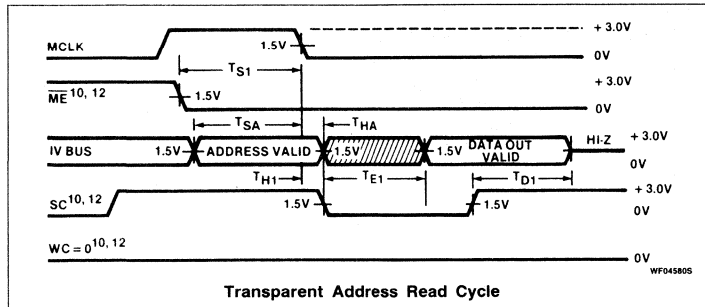
NOTES:

- All voltage values are with respect to network ground terminal.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
- Test each pin one at a time.
- Measured with a logic Low stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with a logic High stored.
- Duration of the short circuit should not exceed 1 second.
- I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V and the output open.
- Minimum required to guarantee a Write into the slowest bit.
- Applied to the 8X300 based system with the data and address pins tied to the IV Bus.
- SC + ME = 1 to avoid bus conflict.
- WC + ME = 1 to avoid bus conflict.
- The SC and WC outputs from the 8X300 are never at 1 simultaneously.
- Measured at Δ of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 500\Omega$, and $C_L = 5pF$.

2K-Bit TTL Bipolar RAM (256 × 8)

8X350

TIMING DIAGRAMS



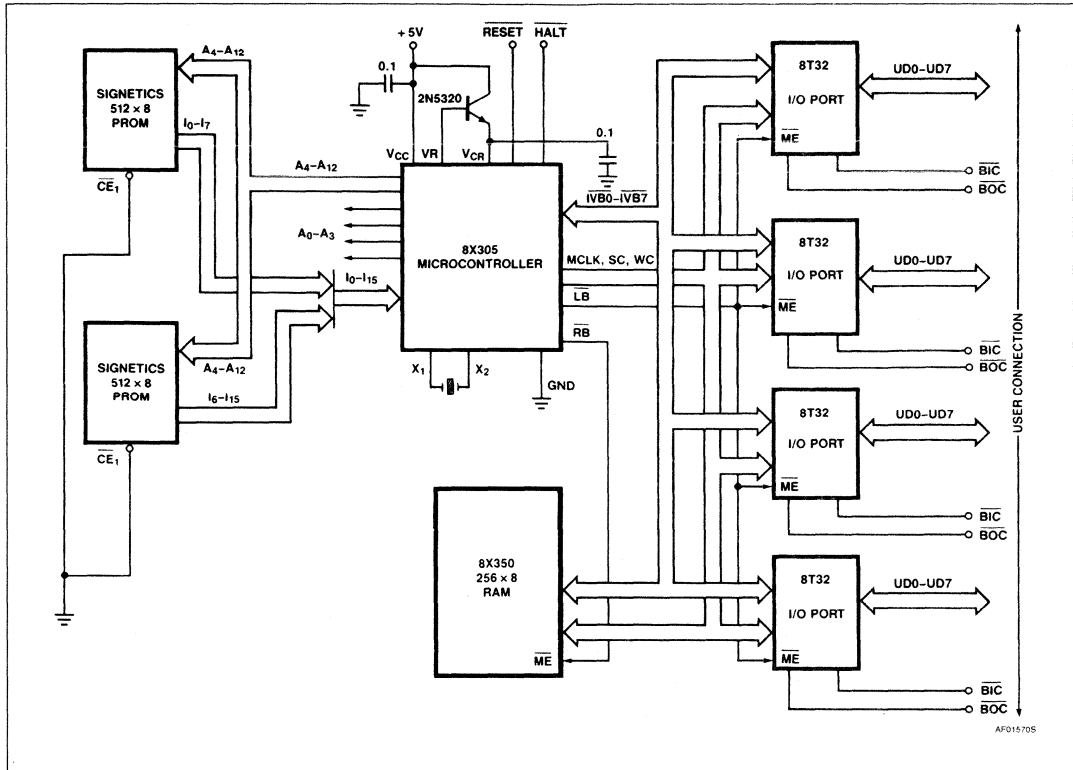
MEMORY TIMING DEFINITIONS

- T_{S1} Required delay between beginning of Master Enable low and falling edge of Master Clock.
- T_{SA} Required delay between beginning of valid address and falling edge of Master Clock.
- T_{HA} Required delay between falling edge of Master Clock and end of valid Address.
- T_{H1} Required delay between falling edge of Master Clock and when Select Command becomes Low.
- T_{E1} Delay between beginning of Select Command low and beginning of valid data output on the IV Bus.
- T_{D1} Delay between when Select Command becomes high and end of valid data output on the IV Bus.
- T_{H2} Required delay between falling edge of Master Clock and when Master Enable becomes Low.
- T_{E2} Delay between when Master Enable becomes low and beginning of valid data output on the IV Bus.
- T_{D2} Delay between when Master Enable becomes high and end of valid data output on the IV Bus.
- T_{S2} Required delay between when Select Command or Write Command becomes Low and when Master Enable becomes Low.
- T_W Minimum width of the Master Clock pulse.
- T_{S3} Required delay between when Master Enable becomes Low and falling edge of Master Clock.
- T_{H3} Required delay between falling edge of Master Clock and when Master Enable becomes High.
- T_{SD} Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
- T_{HD} Required delay between falling edge of Master Clock and end of valid data input on the IV Bus.
- T_{H4} Required delay between falling edge of Master Clock and when Write Command becomes Low.

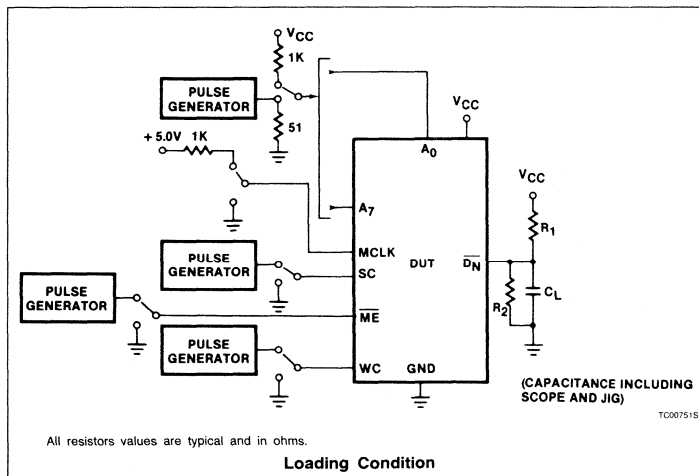
2K-Bit TTL Bipolar RAM (256 × 8)

8X350

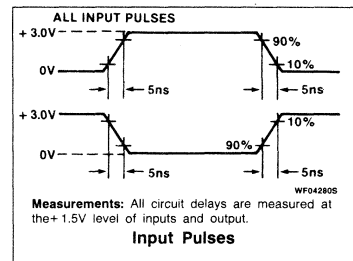
TYPICAL 8X350 APPLICATION



TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROM Programming Information

Generic Programming Procedures	197
--------------------------------------	-----

Bipolar Memory Products

GENERIC I PROGRAMMING

The Signetics family of Advanced Junction Isolated Schottky PROMs are high performance bipolar devices which use a nickel/chromium (NiCr) alloy fuse to provide the many benefits of field programming. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming (except the 82S115 which has two fusing pins: FE1 and FE2). The programming voltages and timing requirements make unintentional programming virtually impossible. Arrays of devices may be programmed in the user's circuit, if desirable, as long as proper application of programming voltages is provided.

GENERIC I PROCEDURE

The Generic I family of Schottky PROMs uses no special pins for programming. The address pins remain TTL compatible during the programming procedure and are used to select the unique word to be programmed. The outputs are used to supply fusing current during the programming mode as well as selection of the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{cc} pin to $8.75 \pm .25V$. This voltage is referred to as V_{ccp} . After the proper delay the output corresponding to the bit selected is raised to $17.5 \pm .5V$. This voltage is known as V_{opf} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{opf} power supply and circuitry. I_{opf} is the current which will be drawn by the part during the programming sequence. Again, after the proper delay the chip enable CE is pulsed to a TTL "0" level for 10 to 25 μs . It is during this time that the actual fusing of the NiCr link occurs. The actual time for fusing of a Signetics NiCr fuse link has been deter-

mined to be between .6 to 1.2 μs . The shorter the fusing pulse (CE), within the recommended limits, the sooner the total programming sequence is completed. Note that unprogrammed Generic I (Junction Isolated) parts are supplied with all bits at a logic "0" level. Only the bits intended to be "ones" will be programmed. Verification of programming can be performed after each bit or after the entire device has been programmed.

A fuse which does not blow during the first programming cycle should be considered a defective device and should be discarded.

GENERIC II PROGRAMMING

The Signetics family of Oxide Isolated Schottky PROMs are high performance bipolar devices which use a vertical diode fuse to provide the benefits of field programming. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming. The programming voltages and timing requirements make unintentional programming virtually impossible.

GENERIC II PROCEDURE

As with the Generic I devices, the addresses remain TTL compatible during the programming procedure and are used to select the unique word to be programmed. The outputs are used to supply fusing current during the programming mode as well as selection of the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{cc} pin to $8.75 \pm .25V$. This voltage is referred to as V_{ccp} . After the proper delay the output corresponding to the bit selected is raised to $20.0 \pm .5V$. This voltage is known as V_{opf} and must be supplied by a voltage source with a low

impedance and very fast transient response. Reliable programming depends on the V_{opf} power supply and circuitry. I_{opf} is the current which will be drawn by the part during the programming sequence. Again, after the proper delay the chip enable CE is pulsed to a TTL "0" level for 1 μs . The properly blown fuse will verify the TTL "0" level. Note that unprogrammed Generic II (Oxide Isolated) parts are supplied with all bits at a logic "1" level. Only the bits intended to be "zeros" will be programmed.

PROGRAMMING INFORMATION

Complete programming system specifications for both Generic I and Generic II products are available upon request from Bipolar Memory Marketing.

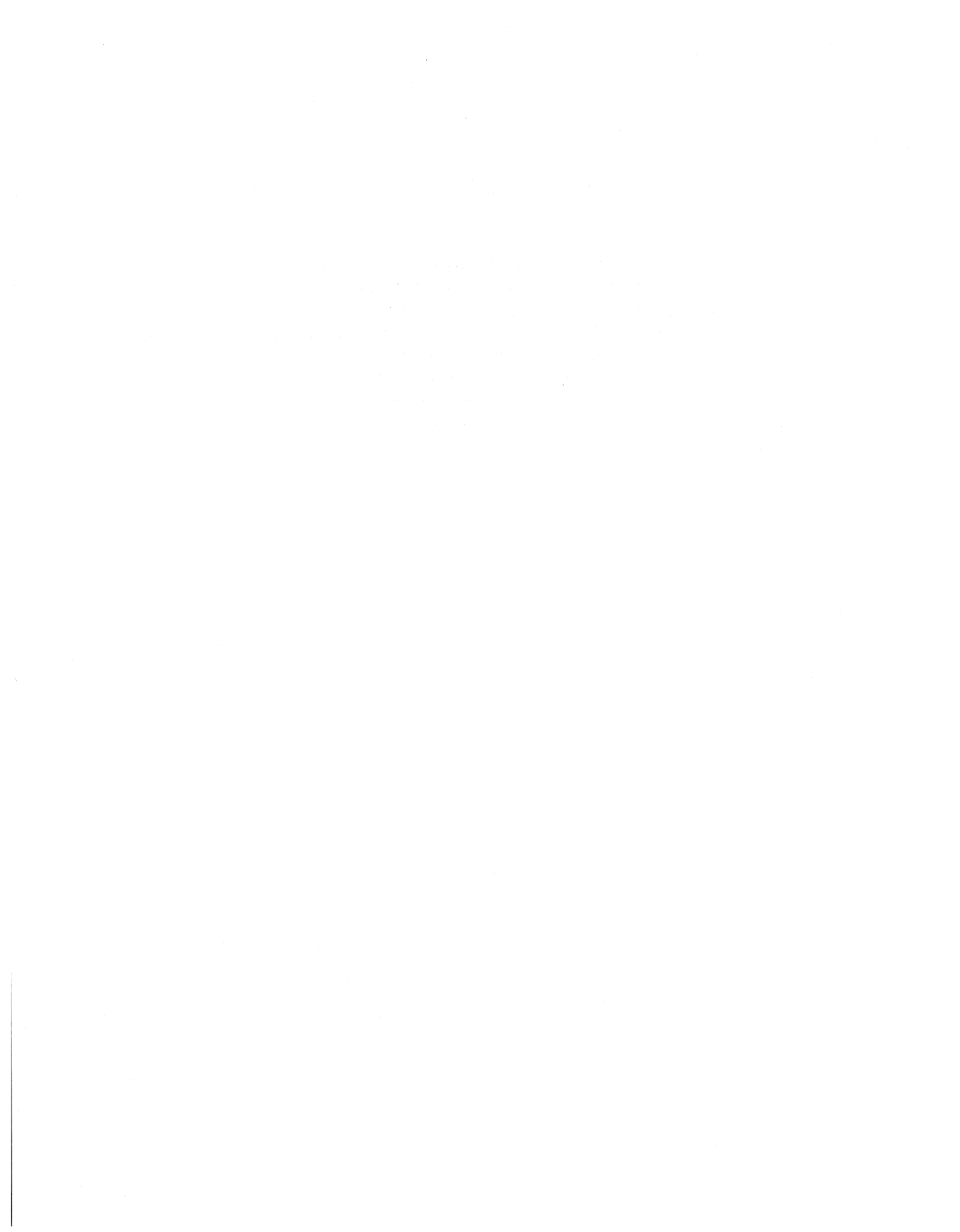
Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available on request from Bipolar Memory Marketing.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT.

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Records of programming yield, by device type, should be kept and any downward trend or sudden change should be considered as an indication of a need to recalibrate the programming equipment.

Low Complexity PROM

82S23/82S123	256-bit Bipolar PROM (32 x 8)201
82S23A/82S123A	256-bit Bipolar PROM (32 x 8)204
82S126/82S129	1024-bit Bipolar PROM (256 x 4)207
82S126A/82S129A	1024-bit Bipolar PROM (256 x 4)210
82S130/82S131	2048-bit Bipolar PROM (512 x 4)213
82S130A/82S131A	2048-bit Bipolar PROM (512 x 4)216
82S135	2048-bit Bipolar PROM (256 x 8)219
82LS135	2048-bit Bipolar PROM (256 x 8)222



82S23 82S123 256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following pages.

The 82S23 and 82S123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

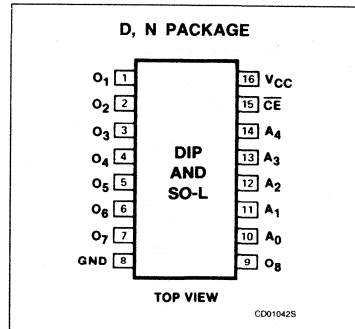
FEATURES

- Address access time: 50ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: $-100\mu\text{A}$ max
- On-chip address decoding
- One chip enable input
- Output options:
 - N82S23: Open collector
 - N82S123: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

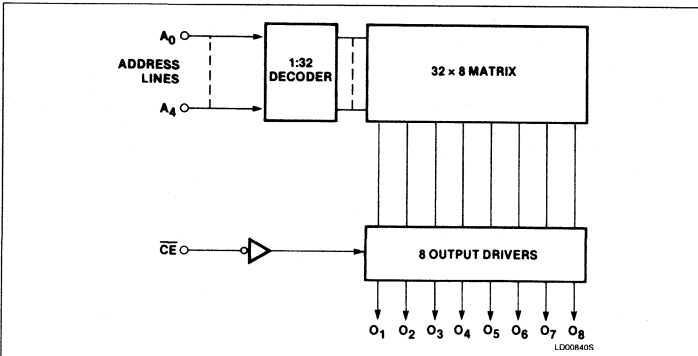
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar PROM (32 × 8)

82S23, 82S123

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S23 N • N82S123 N
Plastic Small Outline 300mil wide 16-pin	N82S23 D • N82S123 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High (82S23) V _O Off-state (82S123)	+5.5	V _{dc}
T _A Temperature range Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High (82S23) V _{IC} Clamp	V _{CC} = 4.75V V _{CC} = 5.25V I _{IN} = -12mA	2.0		0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE} = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 50	μA
Output current I _{OLK} Leakage (82S23) I _{OZ} Hi-Z State (82S123) I _{OS} Short circuit (82S123) ³	\overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = Low, V _{OUT} = 0V, High stored			40 40 -40 -90	μA mA
Supply current I _{CC}	V _{CC} = 5.25V			96	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

256-Bit TTL Bipolar PROM (32 × 8)

82S23, 82S123

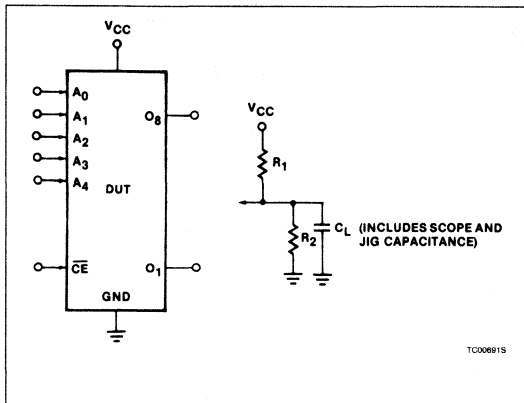
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time ⁴ T_{AA} T_{CE}	Output Output	Address Chip enable		45	50 35	ns
Disable time ⁶ T_{CD}	Output	Chip enable			35	ns

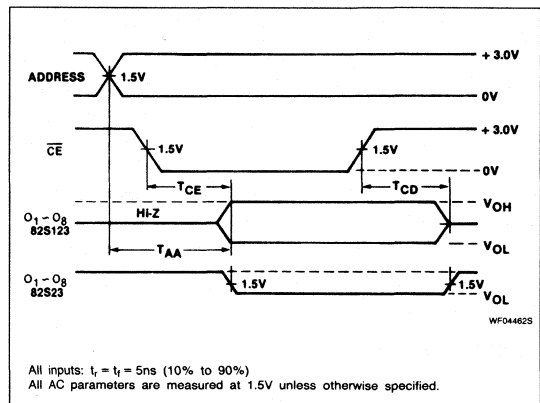
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground terminal.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S23A 82S123A 256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23A and 82S123A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23A and 82S123A devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S23A and 82S123A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

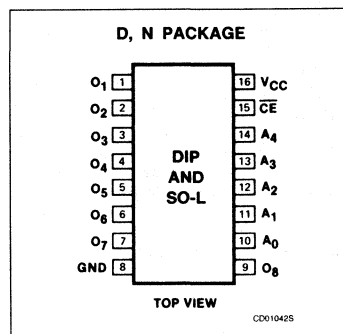
FEATURES

- Address access time: 25ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: $-100\mu\text{A}$ max
- On-chip address decoding
- One chip enable input
- Output options:
 - N82S23A: Open collector
 - N82S123A: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

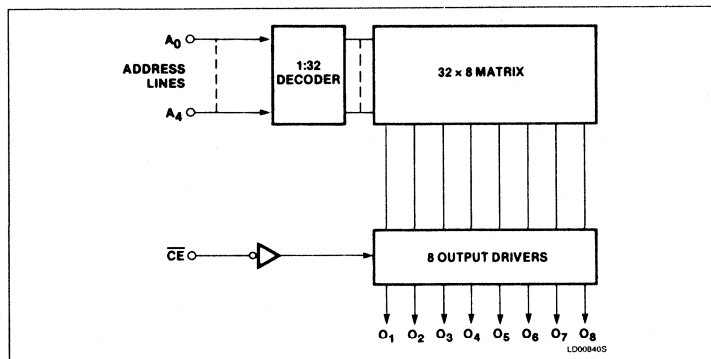
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

PIN CONFIGURATION



LOGIC DIAGRAM



256-Bit TTL Bipolar PROM (32 × 8)

82S23A, 82S123A

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S23A N • N82S123A N
Plastic Small Outline 300mil wide 16-pin	N82S23A D • N82S123A D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	
V _{OH} Output voltage High (82S23A)	+5.5	V _{dc}
V _O Off-state (82S123A)	+5.5	
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0		0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE} = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 50	μA
Output current I _{OLK} Leakage (82S23A) I _{OZ} Hi-Z State (82S123A) I _{OS} Short circuit (82S123A) ³	\overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = Low, V _{OUT} = 0V, High stored	-15		40 40 -40 -90	μA mA
Supply current I _{CC}	V _{CC} = 5.25V			96	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

256-Bit TTL Bipolar PROM (32 × 8)

82S23A, 82S123A

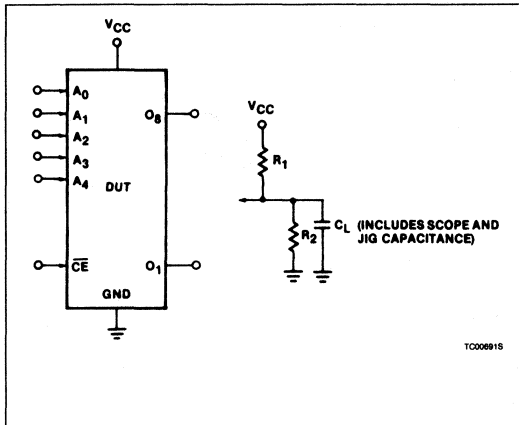
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time T_{AA} ⁴ T_{CE}	Output	Address		20	25	ns
	Output	Chip enable			18	
Disable time ⁶ T_{CD}	Output	Chip disable			18	ns

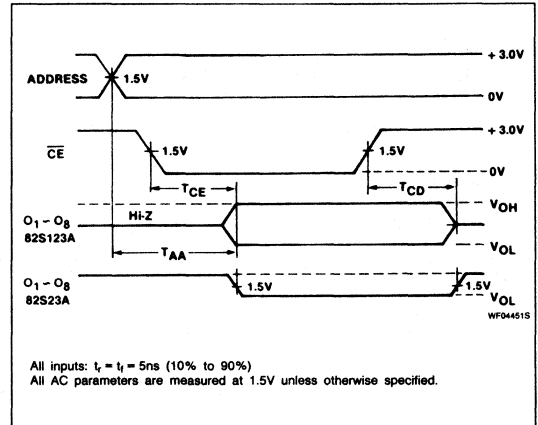
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_C = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750$, $R_2 = 750$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S126 82S129 1K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at logical High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126 and 82S129 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

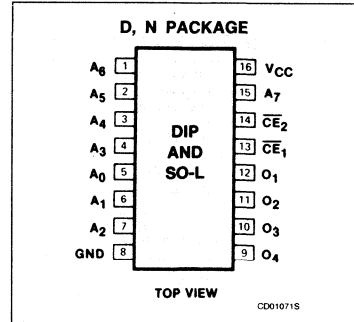
FEATURES

- Address access time: 50ns max
- Power dissipation: 0.5mW/bit typ
- Input loading: $-100\mu\text{A}$ max
- On-chip address decoding
- Two chip enable inputs
- Output options:
 - N82S126: Open collector
 - N82S129: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

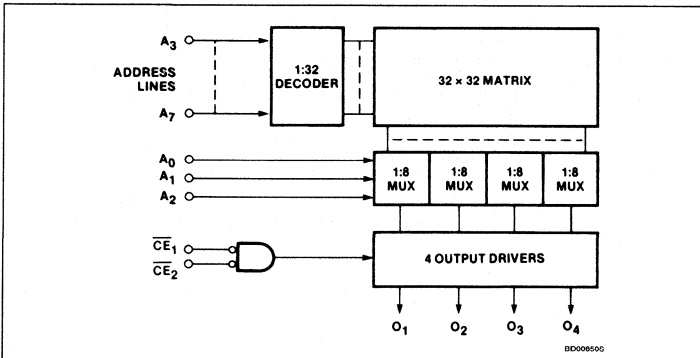
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit TTL Bipolar PROM (256 × 4)

82S126, 82S129

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S126 N • N82S129 N
Plastic Small Outline 300mil wide 16-pin	N82S126 D • N82S129 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} Supply voltage	+7	V_{dc}
V_{IN} Input voltage	+5.5	V_{dc}
V_{OH} Output voltage High (82S126)	+5.5	V_{dc}
V_O Off-state (82S129)	+5.5	
T_A Operating T_{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V_{IL} Low V_{IH} High V_{IC} Clamp	$I_{IN} = -12\text{mA}$	2.0		0.8 -1.2	V
Output voltage V_{OL} Low V_{OH} High (82S129)	$\overline{CE}_{1,2} = \text{Low}$ $I_{OUT} = 16\text{mA}$ $I_{OUT} = -2.0\text{mA}$	2.4		0.45	V
Input current I_{IL} Low I_{IH} High	$V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-100 40	μA
Output current I_{OLK} Leakage (82S126) I_{OZ} Hi-Z State (82S129) I_{OS} Short circuit (82S129) ³	\overline{CE}_1 or $\overline{CE}_2 = \text{High}$, $V_{OUT} = 5.5\text{V}$ \overline{CE}_1 or $\overline{CE}_2 = \text{High}$, $V_{OUT} = 5.5\text{V}$ \overline{CE}_1 or $\overline{CE}_2 = \text{High}$, $V_{OUT} = 0.5\text{V}$ $\overline{CE}_{1,2} = \text{Low}$, $V_{OUT} = 0\text{V}$, Stored High			40 40 -40 -70	μA mA
Supply current I_{CC}	$V_{CC} = 5.25\text{V}$			120	mA
Capacitance C_{IN} Input C_{OUT} Output	\overline{CE}_1 or $\overline{CE}_2 = \text{High}$, $V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8		pF

1K-Bit TTL Bipolar PROM (256 × 4)

82S126, 82S129

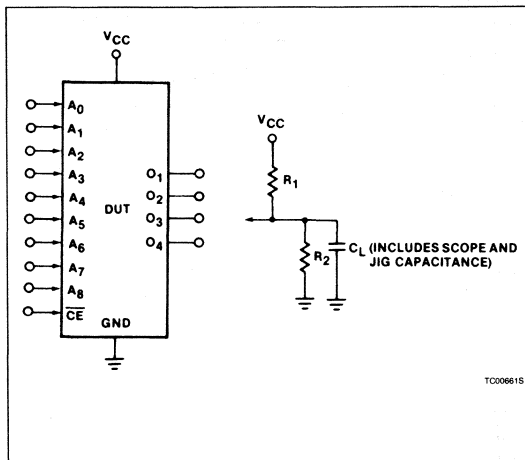
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	MIN	TYP ⁵	MAX	UNIT
Access time⁴ T_{AA} T_{CE}	Output Output	Address Chip enable		40	50 25	ns
Disable time⁶ T_{CD}	Output	Chip disable			25	ns

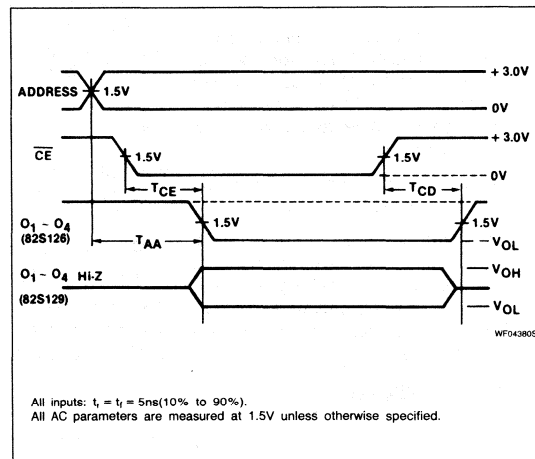
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S126A 82S129A 1K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S126A and 82S129A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126A and 82S129A devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126A and 82S129A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

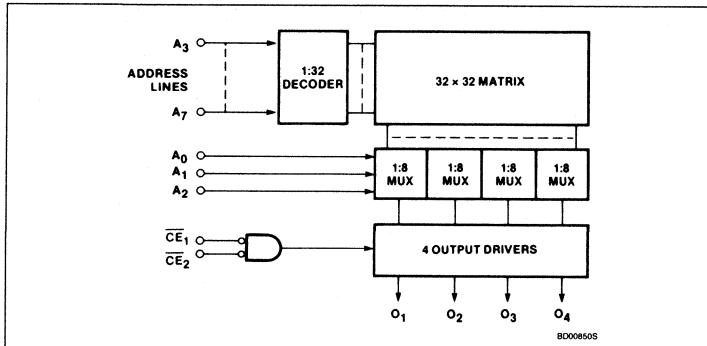
FEATURES

- Address access time:
 - 82S126A: 30ns max
 - 82S129A: 27ns max
- Power dissipation: 0.5mW/bit typ
- Input loading: $-100\mu\text{A}$ max
- On-chip address decoding
- Two Chip Enable Inputs
- Output options:
 - 82S126A: Open collector
 - 82S129A: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

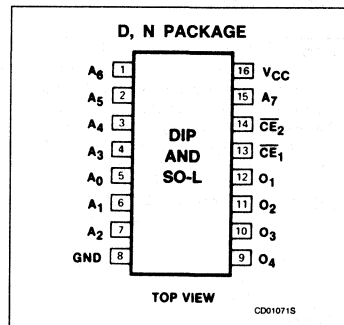
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATION



1K-Bit TTL Bipolar PROM (256 × 4)

82S126A, 82S129A

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S126A N • N82S129A N
Plastic Small Outline 300mil wide 16-pin	N82S126A D • N82S129A D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High (82S126)	+5.5	V _{dc}
V _O Off-state (82S129)	+5.5	
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	V _{CC} = 4.75V V _{CC} = 5.25V V _{CC} = 4.75V, I _{IN} = -12mA	2.0		0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High (82S129A)	$\overline{CE}_{1,2}$ = Low I _{OUT} = 16mA I _{OUT} = -2.0mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OLK} Leakage (82S126A) I _{OZ} Hi-Z State (82S129A) I _{OS} Short circuit (82S129A) ³	\overline{CE}_1 or \overline{CE}_2 = High, V _{OUT} = 5.5V \overline{CE}_1 or \overline{CE}_2 = High, V _{OUT} = 5.5V \overline{CE}_1 or \overline{CE}_2 = High, V _{OUT} = 0.5V $\overline{CE}_{1,2}$ = Low, V _{OUT} = 0V, Stored High	-15		40 40 -40 -70	μA mA
Supply current ³ I _{CC}	V _{CC} = 5.25V			120	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE}_1 or \overline{CE}_2 = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

1K-Bit TTL Bipolar PROM (256 × 4)

82S126A, 82S129A

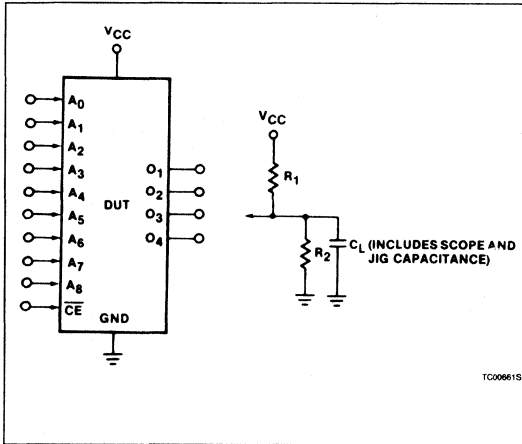
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S129A			N82S126A			UNIT
			Min	Typ ⁵	Max	Min	Typ ⁵	Max	
Access time ⁴ T_{AA} T_{CE}	Output	Address		17	27		17	30	ns
		Chip enable		10	20		10	20	
Disable time ⁶ T_{CD}	Output	Chip enable		6	15		6	15	ns

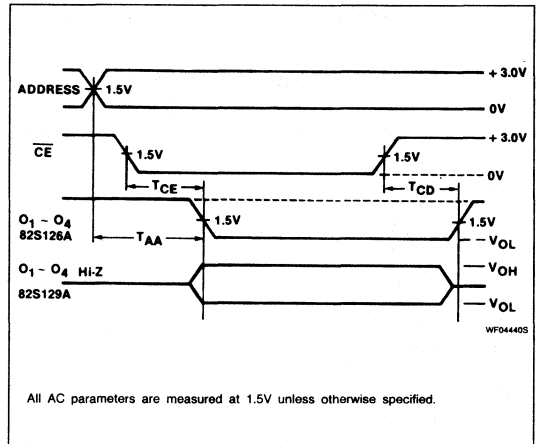
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S130 82S131 2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130 and 82S131 are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S130 and 82S131 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

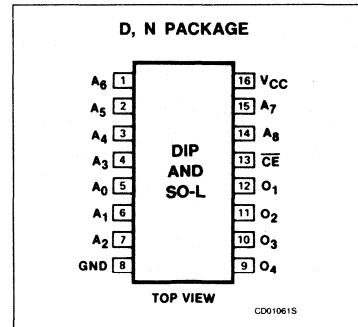
FEATURES

- Address access time: 50ns max
- Power dissipation: 0.3mW/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- One chip enable input
- Output options:
 - N82S130: Open collector
 - N82S131: Three-state
- No separate fusing-pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

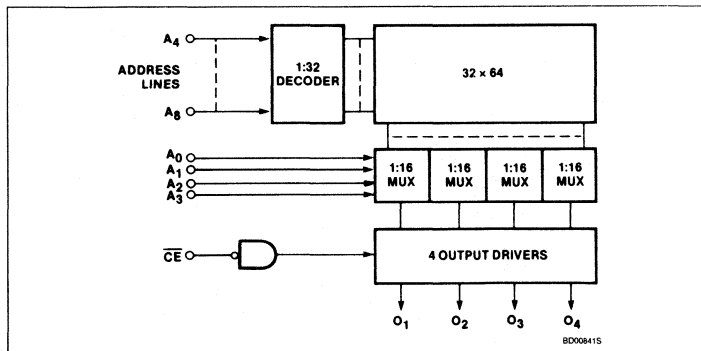
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (512 × 4)

82S130, 82S131

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S130 N • N82S131 N
Plastic Small Outline 300mil wide 16-pin	N82S130 D • N82S131 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High (82S130)	+5.5	V _{dc}
V _O Off-state (82S131)	+5.5	
T _A Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	0.8	-1.2	V
Output voltage V _{OL} Low V _{OH} High (82S131)	\overline{CE} = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OLK} Leakage (82S130) I _{OZ} Hi-Z State (82S131) I _{OS} Short circuit (82S131) ³	\overline{CE} = High, V _{OUT} = 5.5V, \overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = Low, V _{OUT} = 0V, Stored High	-15		40 40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V			140	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

2K-Bit TTL Bipolar PROM (512 × 4)

82S130, 82S131

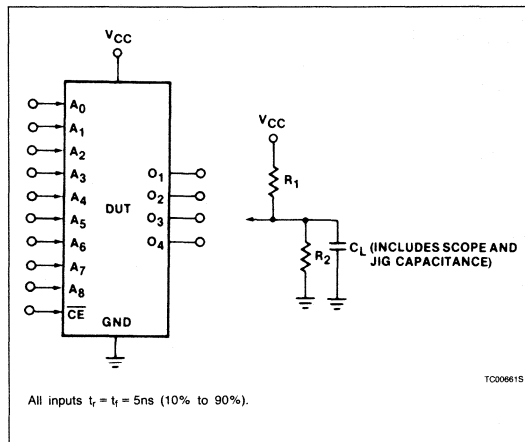
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address Chip enable			50 30	ns
Disable time⁶ T_{CD}	Output	Chip disable			30	ns

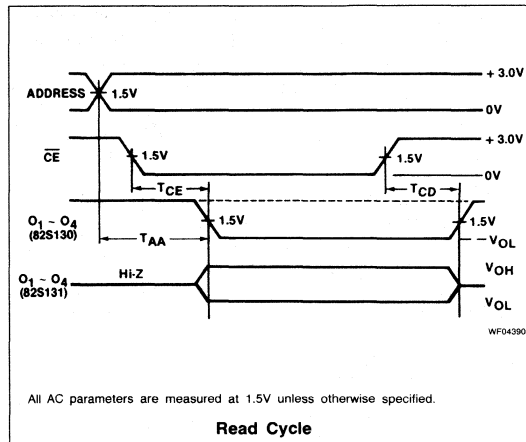
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All AC parameters are measured at 1.5V unless otherwise specified.

82S130A 82S131A 2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S130A and 82S131A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130A and 82S131A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S130A and 82S131A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

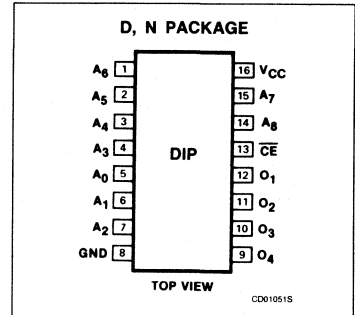
FEATURES

- Address access time:
 - N82S130A: 33ns max
 - N82S131A: 30ns max
- Power dissipation: 0.3mW/bit typ
- Input loading: $-100\mu A$ max
- On-chip address decoding
- One chip enable input
- Output options:
 - N82S130A: Open collector
 - N82S131A: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

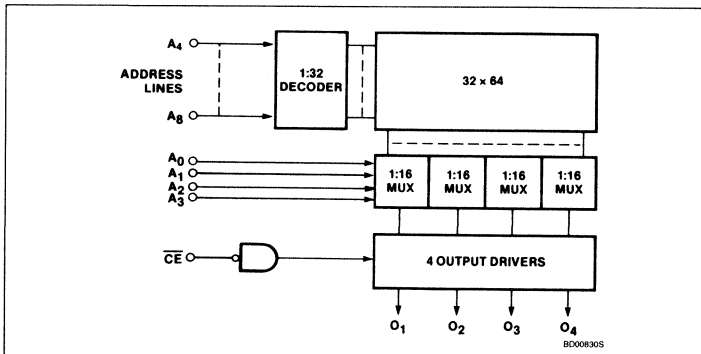
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (512 × 4)

82S130A, 82S131A

ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual Inline 300mil wide 16-pin	N82S130A N • N82S131A N
Plastic Small Outline 300 mil wide 16-pin	N82S130A D • N82S131A D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High (82S130)	+5.5	V _{dc}
V _O Off-state (82S131)	+5.5	
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage					
V _{IL} Low				0.8	V
V _{IH} High		2.0			
V _{IC} Clamp	I _{IN} = -12mA			-1.2	
Output voltage					
V _{OL} Low	\overline{CE} = Low I _{OUT} = 16mA			0.45	V
V _{OH} High (82S131)	I _{OUT} = -2mA	2.4			
Input current					
I _{IL} Low	V _{IN} = 0.45V			-100	μA
I _{IH} High	V _{IN} = 5.5V			40	
Output current					
I _{OLK} Leakage (82S130A)	\overline{CE} = High, V _{OUT} = 5.5V			40	μA
I _{OZ} Hi-Z State (82S131A)	\overline{CE} = High, V _{OUT} = 5.5V			40	
	\overline{CE} = High, V _{OUT} = 0.5V			-40	
I _{OS} Short circuit (82S131A) ³	\overline{CE} = Low, V _{OUT} = 0V, Stored High	-15		-70	mA
Supply current					
I _{CC}	V _{CC} = 5.25V			140	mA
Capacitance					
C _{IN} Input	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V		5		pF
C _{OUT} Output	V _{OUT} = 2.0V		8		

2K-Bit TTL Bipolar PROM (512 × 4)

82S130A, 82S131A

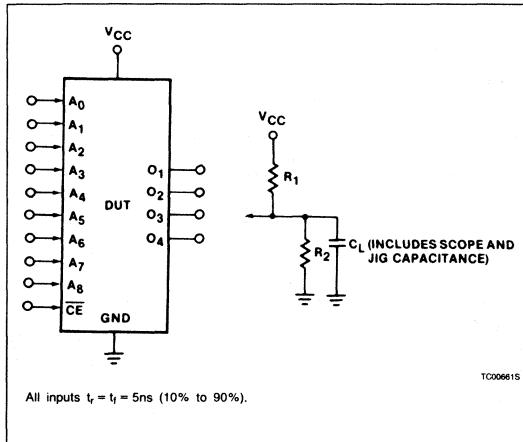
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	N82S131A			N82S130A			UNIT
			Min	Typ ⁵	Max	Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address		18	30		18	33	ns
		Chip enable		10	20		10	20	ns
Disable time⁶ T_{CD}	Output	Chip enable		6	15		6	15	ns

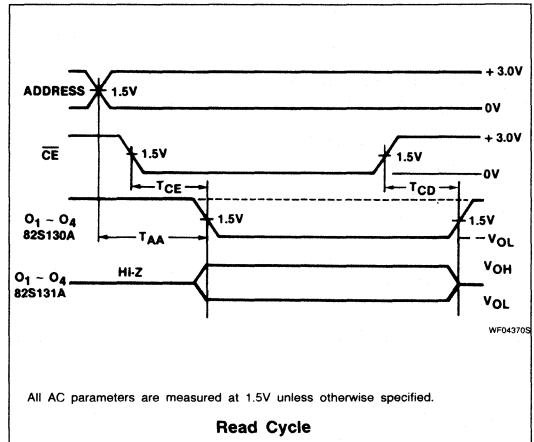
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S135 2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S135 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S135 includes on-chip decoding and two chip enable inputs for ease of memory expansion, and features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S135 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

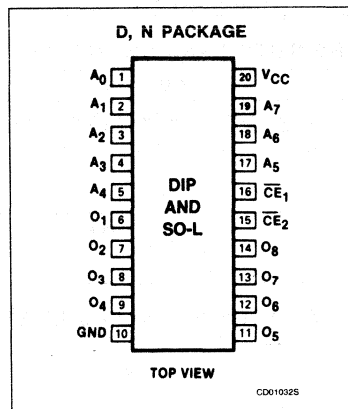
FEATURES

- Address access time: 45ns max
- Power dissipation: 329 μ W/bit typ
- Input loading: -100 μ A max
- Two chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Outputs: Three-state
- Unprogrammed outputs are Low level

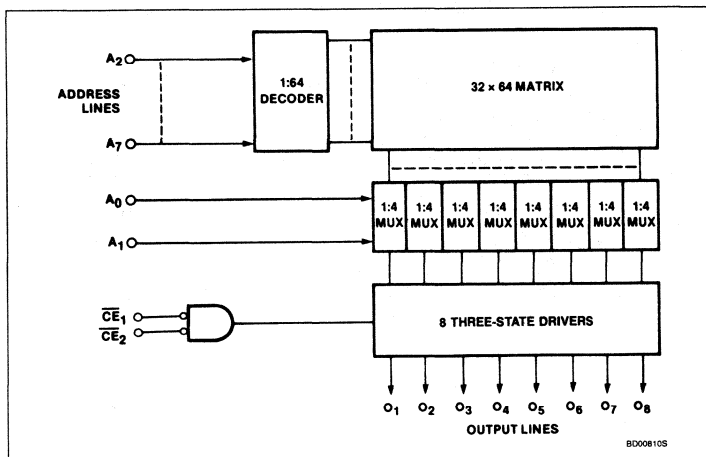
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (256 × 8)

82S135

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 20-pin	N82S135 N
Plastic Small Outline 300mil wide 20-pin	N82S135 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	V _{CC} = 4.75V V _{CC} = 5.25V I _{IN} = -12mA	2.0		.80 -1.2	V
Output voltage V _{OL} Low V _{OH} High	I _{OUT} = 9.6mA C _{E1} , C _{E2} = Low, I _{OUT} = -2mA, High stored	2.4		.50	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ³	C _{E1} , C _{E2} = High, V _{OUT} = 0.5V C _{E1} , C _{E2} = High, V _{OUT} = 5.5V C _{E1} , C _{E2} = Low, V _{OUT} = 0V, One Stored	-15		-40 40 -75	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		135	150	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V, C _E = High V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

2K-Bit TTL Bipolar PROM (256 × 8)

82S135

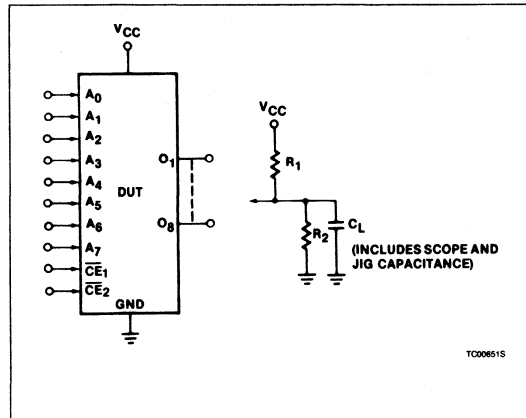
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output Output	Address Chip enable		40 20	45 25	ns
Disable time⁶ T_{CD}	Output	Chip disable		20	35	ns

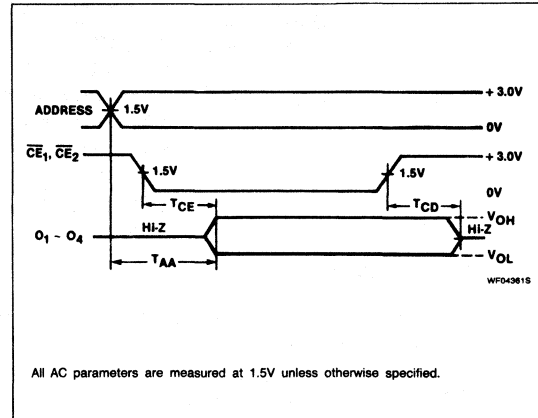
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All AC parameters are measured at 1.5V unless otherwise specified.

82LS135 2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LS135 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two chip enable inputs for ease of memory expansion, and features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

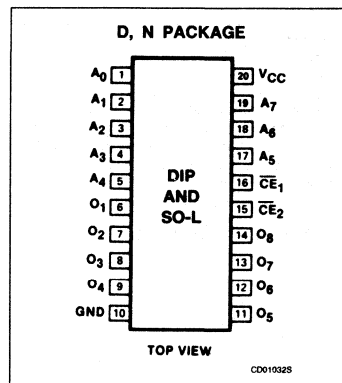
FEATURES

- Address access time: 100ns max.
- Power dissipation: 200 μ W/bit typ
- Input loading: -100 μ A max
- Two chip enable inputs
- On chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Unprogrammed outputs are at Low level
- Outputs: Three-state

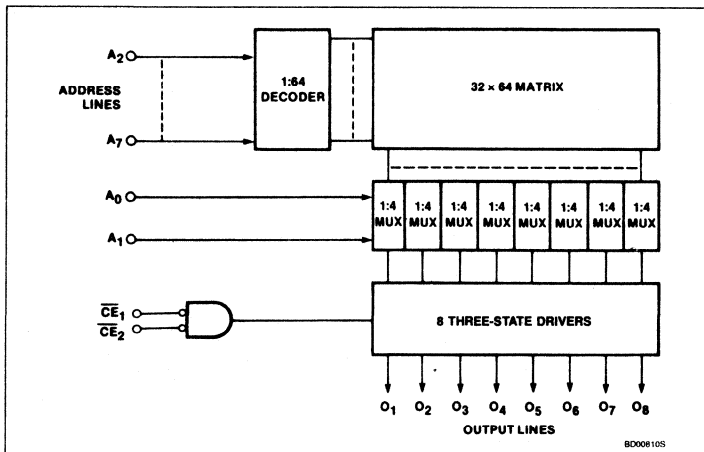
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (256 × 8)

82LS135

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 20-pin	N82LS135 N
Plastic Small Outline 300mil wide 20-pin	N82LS135 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0		.80 -1.2	V
Output voltage V _{OL} Low V _{OH} High	I _{OUT} = 16mA I _{OUT} = -2mA, High stored	2.4		.50	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IH} = 5.5V			100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ³	$\overline{CE}_1, \overline{CE}_2 = \text{High}, V_{OUT} = 0.5V$ $\overline{CE}_1, \overline{CE}_2 = \text{High}, V_{OUT} = 5.5V$ $\overline{CE}_1, \overline{CE}_2 = \text{Low}, V_{OUT} = 0V, \text{One stored}$	-15		-40 40 -75	μA ma
Supply current I _{CC}	V _{CC} = 5.25V		80	100	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V $\overline{CE} = \text{High}$ V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

2K-Bit TTL Bipolar PROM (256 × 8)

82LS135

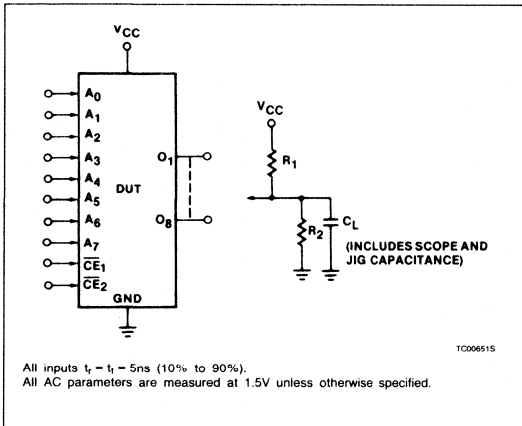
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ₅	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address		70	100	ns
	Output	Chip enable		30	50	
Disable time⁶ T_{CD}	Output	Chip disable		30	60	ns

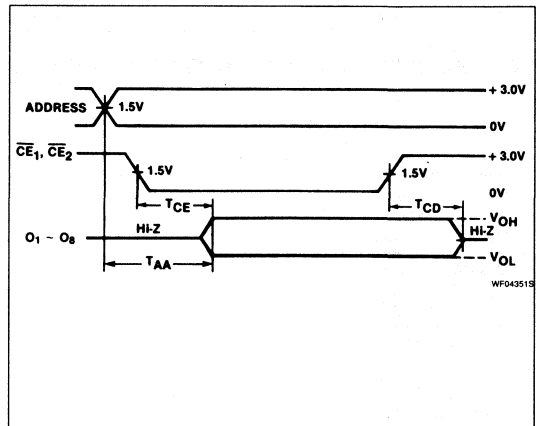
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



4K-bit TTL Bipolar PROM

82S115	4096-bit PROM (512 x 8).....	.227
82S137	4096-bit PROM (1024 x 4).....	.231
82S137A/82S137B	4096-bit PROM (1024 x 4).....	.234
82S147/82S147A	4096-bit PROM (512 x 8).....	.237

82S115 4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the Three-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the bit drivers will be controlled solely by \overline{CE}_1 and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (High, Low, or High Z) as long as Strobe is Low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the High Z State if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled,

or causes outputs to be locked into the High Z condition if the chip was disabled.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

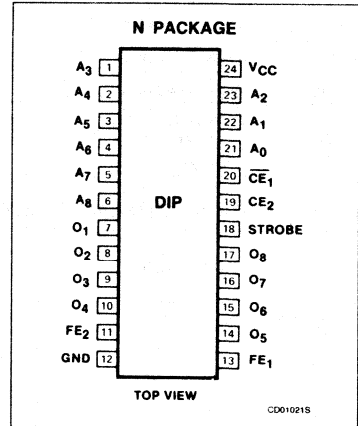
FEATURES

- Address access time: 60ns max
- Power dissipation: 165 μ W/bit typ
- Input loading: -100 μ A max
- On-chip storage latches
- Schottky clamped
- Fully TTL compatible
- Outputs: Three-state

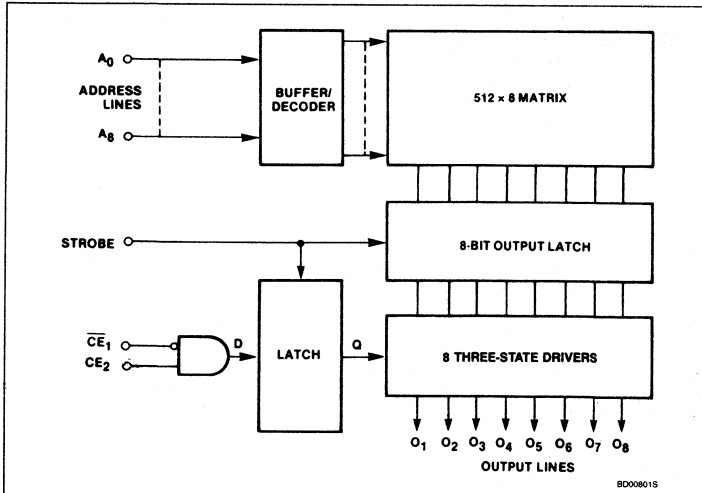
APPLICATIONS

- Microprogramming
- Hardware algorithms
- Character generation
- Control store
- Sequential controllers

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (512 × 8)

82S115

ORDERING CODE

DESCRIPTION	ORDERING CODES
Plastic Dual Inline 600mil wide 24-pin	N82S115 N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
T _A Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ⁵	LIMITS			UNIT
		Min	Typ ⁸	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE}_1 = Low, CE ₂ = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.7	0.4	0.45	V
Input current⁵ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 25	μA
Output current⁵ I _{OZ} Hi-Z State I _{OS} Short circuit ¹	\overline{CE}_1 = High or CE ₂ = Low, V _{OUT} = 5.5V \overline{CE}_1 = High or CE ₂ = Low, V _{OUT} = 0.5V \overline{CE}_1 = Low, CE ₂ = High, V _{OUT} = 0V, High stored	-15		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		130	175	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE}_1 = High or CE ₂ = Low, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

4K-Bit TTL Bipolar PROM (512 × 8)

82S115

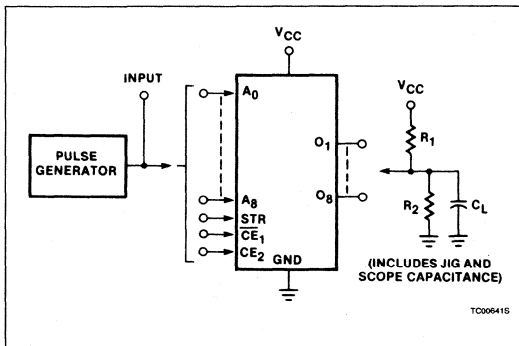
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega, R_2 = 1k\Omega, C_L = 30pF, 0^\circ \leq T_A \leq +75^\circ C, 4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT		
				Min	Typ ⁸	Max			
Access time ⁶ T_{AA} T_{CE}	Output Output	Address Chip enable	Latched or transparent Read ^{2,4}		40 20	60 40	ns		
Disable time ⁹ T_{CD}	Output	Chip disable			20	40		ns	
Set-up and hold time T_{CDS} Set-up time T_{CDH} Hold time	Output	Chip enable	Latched Read only ^{3,4}	40 10			ns		
Hold time T_{ADH} Hold time	Address	Strobe			0				
Pulse Width T_{SW} Strobe					30	15		ns	
Latch time T_{SL} Strobe					60	35		ns	
Delatch time ⁹ T_{DL} Strobe								35	ns

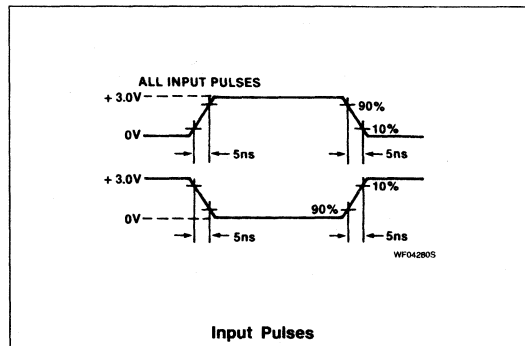
NOTES:

- No more than one output should be grounded at the same time and strobe should be disabled Strobe is in the High state.
- If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or High impedance state after it has been enabled.
- In latched Read Mode data from any selected address will be held on the output when Strobe is lowered only when Strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
- During operation the fusing pins FE_1 and FE_2 may be grounded or left floating.
- Positive current is defined as into the terminal referenced.
- Tested at an address cycle time of 1 μ sec.
- Areas shown by crosshatch are latched data from previous address.
- Typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.
- Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega, R_2 = 750\Omega$, and $C_L = 5pF$.

TEST LOAD CIRCUIT



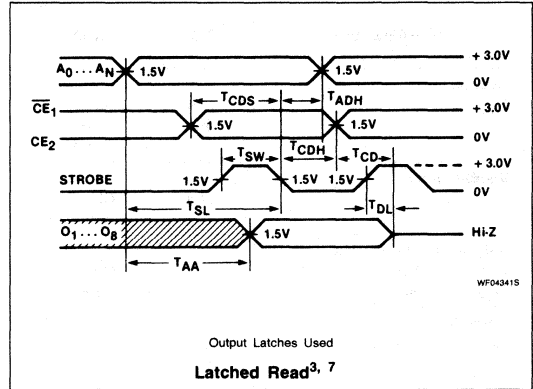
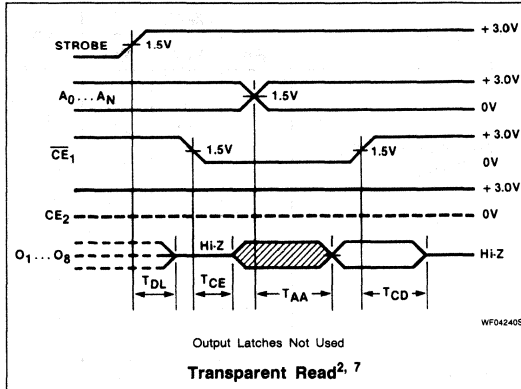
VOLTAGE WAVEFORM



4K-Bit TTL Bipolar PROM (512 × 8)

82S115

TIMING DIAGRAMS



82S137 4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S137 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S137 devices are also processed to military requirements for operation over the military temperature range, for specifications and ordering information consult the Signetics Military Data Book.

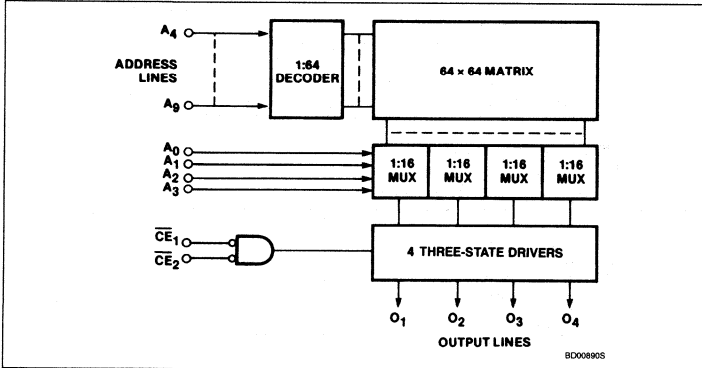
FEATURES

- Address access time: 60ns max
- Power dissipation: .13mW/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Two chip enable inputs
- Outputs: Three-state

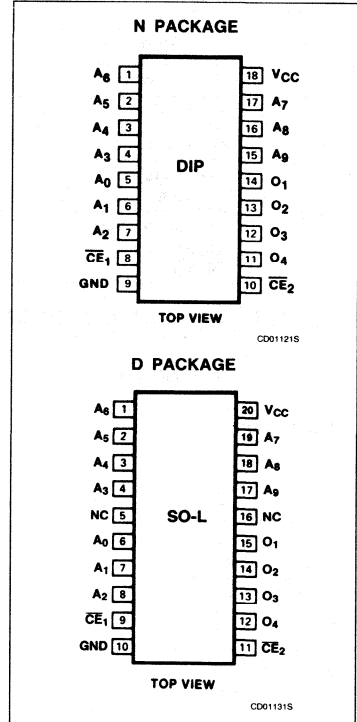
APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATION



4K-Bit TTL Bipolar PROM (1024 × 4)

82S137

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 18-pin	N82S137 N
Plastic Small Outline 300mil wide 20-pin	N82S137 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0		0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	$\overline{CE}_{1,2}$ = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ³	$\overline{CE}_{1,2}$ = High, V _{OUT} = 0.5V $\overline{CE}_{1,2}$ = High, V _{OUT} = 5.5V $\overline{CE}_{1,2}$ = Low, V _{OUT} = 0V, Stored High	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V			140	mA
Capacitance C _{IN} Input C _{OUT} Output	$\overline{CE}_{1,2}$ = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

4K-Bit TTL Bipolar PROM (1024 × 4)

82S137

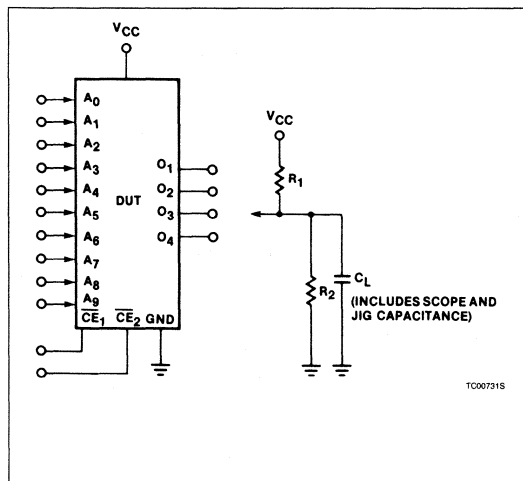
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address		40	60	ns
	Output	Chip enable		25	30	
Disable time⁶ T_{CD}	Output	Chip enable		25	30	ns

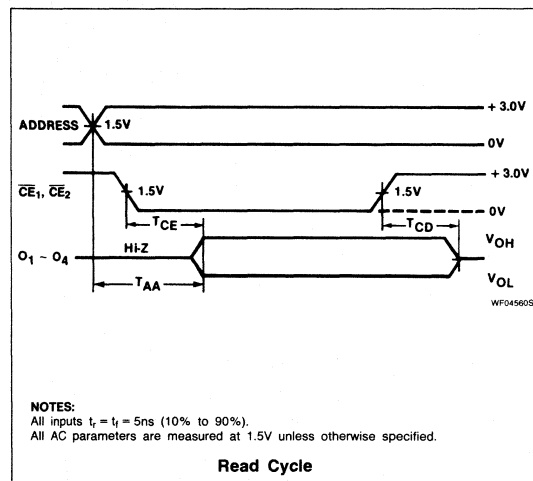
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S137A 82S137B 4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

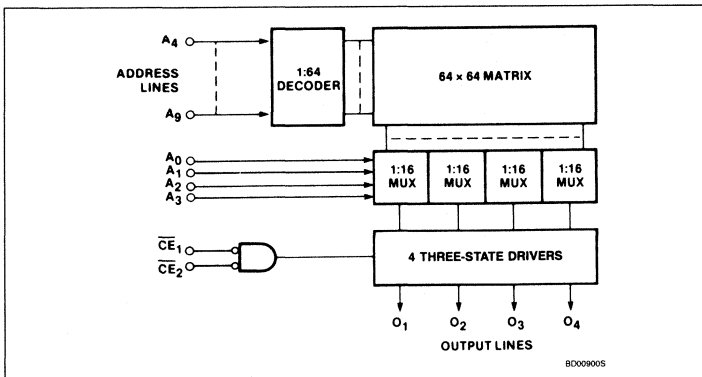
The 82S137A and 82S137B are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137A and 82S137B are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S137A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

BLOCK DIAGRAM



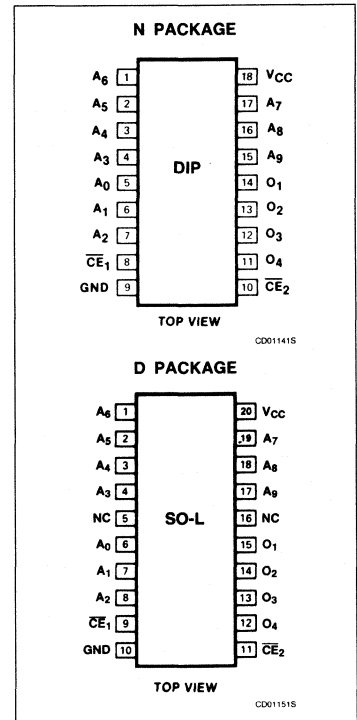
FEATURES

- Address access time:
 - N82S137A: 45ns max
 - N82S137B: 35ns max
- Power dissipation: .13mW/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Two chip enable inputs
- Outputs: Three-state

APPLICATIONS

- Control store
- Sequential controllers
- Random logic
- Code conversion

PIN CONFIGURATION



4K-Bit TTL Bipolar PROM (1024 × 4)

82S137A, 82S137B

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 18-pin	N82S137A N • N82S137B N
Plastic Small Outline 300mil wide 20-pin	N82S137A D • N82S137B D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	$\overline{CE}_{1,2}$ = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ³	$\overline{CE}_{1,2}$ = High, V _{OUT} = 0.5V $\overline{CE}_{1,2}$ = High, V _{OUT} = 5.5V $\overline{CE}_{1,2}$ = Low, V _{OUT} = 0V, Stored High	-15		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		85	140	mA
Capacitance C _{IN} Input C _{OUT} Output	$\overline{CE}_{1,2}$ = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

4K-Bit TTL Bipolar PROM (1024 × 4)

82S137A, 82S137B

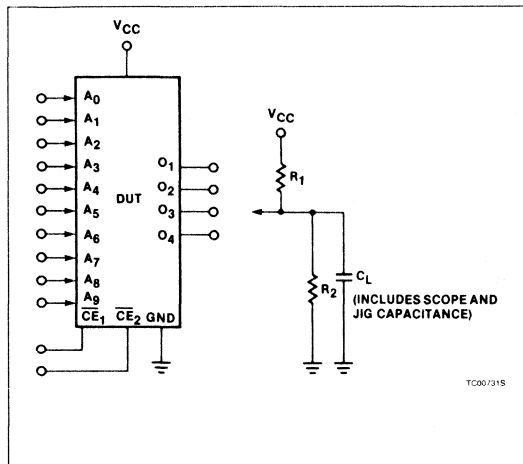
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	N82S137A			N82S137B			UNIT
			Min	Typ ⁵	Max	Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address Chip enable		35 20	45 30		30 15	35 25	ns
Disable time⁶ T_{CD}	Output	Chip disable		20	30		15	25	ns

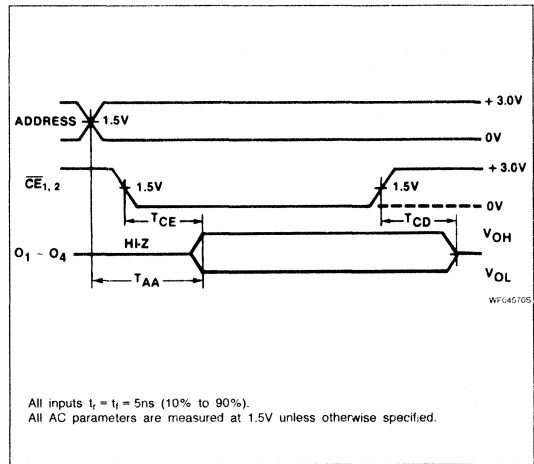
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S147 82S147A 4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S147 and 82S147A are field-programmable, which means that custom patterns are immediately available by following the Signetics generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147 and 82S147A includes on-chip decoding and one chip enable input for ease of memory expansion, and features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S147 and 82S147A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

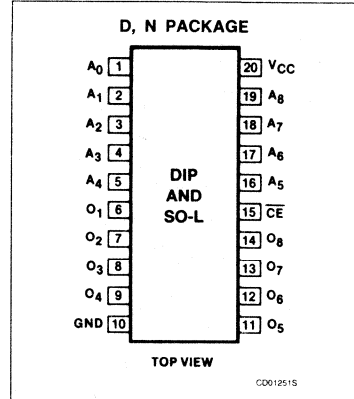
FEATURES

- Address access time:
 - N82S147: 60ns max
 - N82S147A: 45ns max
- Power dissipation: 625mW typ
- Input loading: -100 μ A max
- One chip enable input
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- One chip enable input
- Outputs: Three-state
- Unprogrammed outputs are Low level

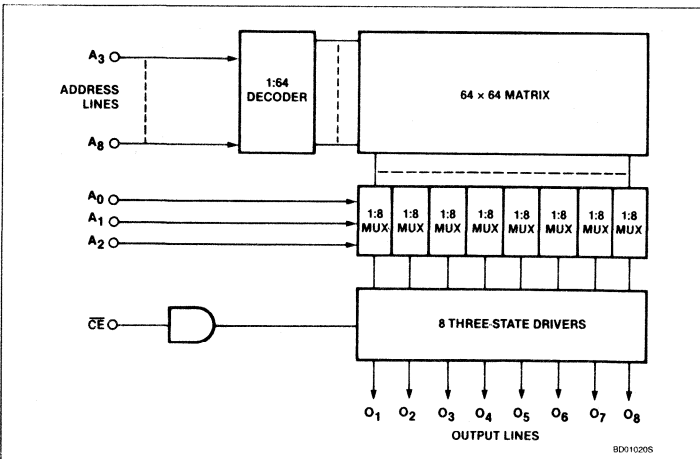
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit Bipolar PROM (512 × 8)

82S147, 82S147A

ORDERING CODE

PACKAGES	ORDER CODES
Plastic Dual Inline 300mil wide 20-pin	N82S147 N • N82S147A N
Plastic Small Outline 300mil wide 20-pin	N82S147 D • N82S147A D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE} = Low I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{oz} Hi-Z State I _{os} Short circuit ³	\overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = Low, V _{OUT} = 0V	-15		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		125	155	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

4K-Bit Bipolar PROM (512 × 8)

82S147, 82S147A

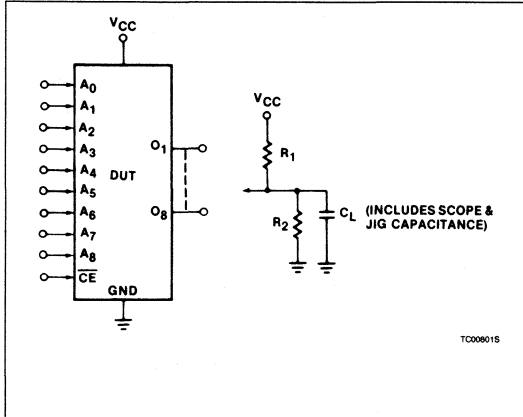
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S147			N82S147A			UNIT
			Min	Typ ⁵	Max	Min	Typ ⁵	Max	
Access time ⁴ T_{AA} T_{CE}	Output Output	Address Chip Enable		45	60		40	45	ns
				20	35		20	30	
Disable time ⁶ T_{CD}	Output	Chip disable		20	35		20	30	ns

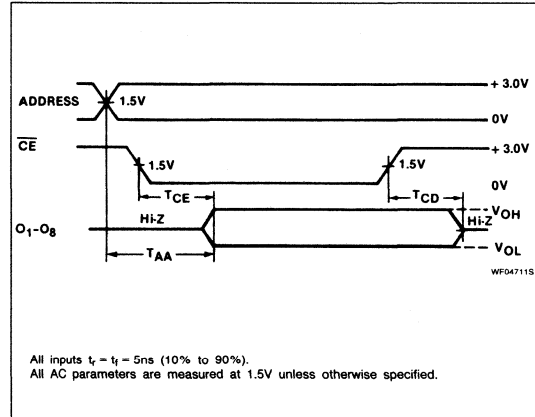
NOTES:

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8K-bit TTL Bipolar PROM

82S181	8192-bit PROM (1024 x 8)	243
82S181C	8192-bit PROM (1024 x 8)	246
82LS181	8192-bit PROM (1024 x 8)	249
82S183	8192-bit PROM (1024 x 8)	252
82S185	8192-bit PROM (2048 x 4)	256
82S185A/82S185B	8192-bit PROM (2048 x 4)	259
82HS187/82HS187A	8192-bit PROM (1024 x 8)	262
82HS189/82HS189A	8192-bit PROM (1024 x 8)	266

82S181 8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

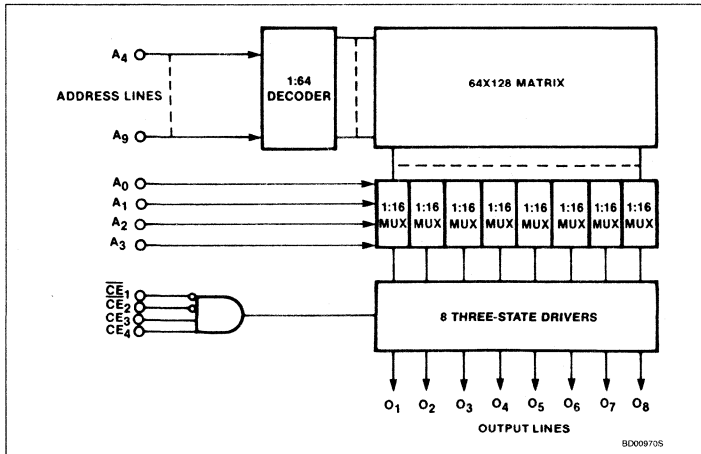
The 82S181 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

BLOCK DIAGRAM



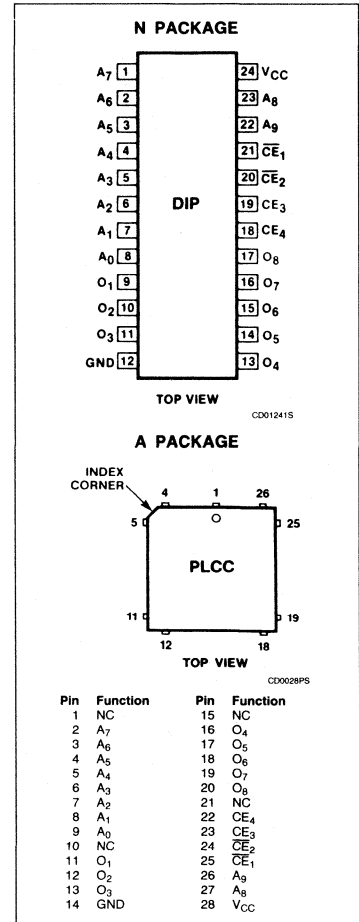
FEATURES

- Address access time: 70ns max
- Power dissipation: 76μW/bit typ
- Input loading: -100μA max
- On-chip address decoding
- Four chip enable inputs
- Outputs: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



8K-Bit TTL Bipolar PROM (1024 × 8)

82S181

ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82S181 N
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82S181 A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage² V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage² V _{OL} Low V _{OH} High	$\overline{CE}_{1,2}$ = Low, CE _{3,4} = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current¹ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current¹ I _{OZ} Hi-Z State I _{OS} Short circuit	$\overline{CE}_{1,2}$ = High, CE _{3,4} = Low, V _{OUT} = 5.5V $\overline{CE}_{1,2}$ = High, CE _{3,4} = Low, V _{OUT} = 0.5V $\overline{CE}_{1,2}$ = Low, CE _{3,4} = High, V _{OUT} = 0V High Stored	-15		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		125	175	mA
Capacitance C _{IN} Input C _{OUT} Output	$\overline{CE}_{1,2}$ = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

8K-Bit TTL Bipolar PROM (1024 × 8)

82S181

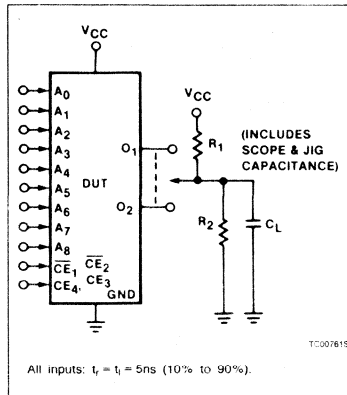
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access Time 4 T_{AA} T_{CE}	Output	Address		50	70	ns
	Output	Chip enable		20	40	
Disable time⁶ T_{CD}	Output	Chip disable		20	40	ns

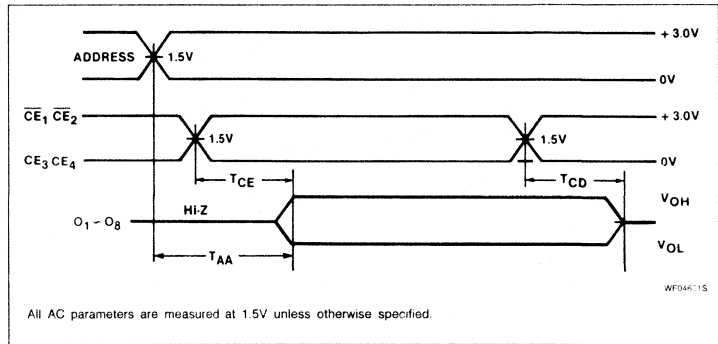
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S181C

8K-Bit TTL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

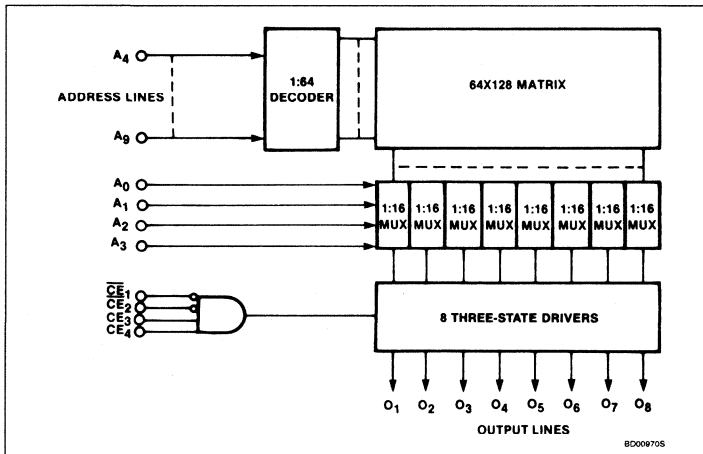
The 82S181C is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181C is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

BLOCK DIAGRAM



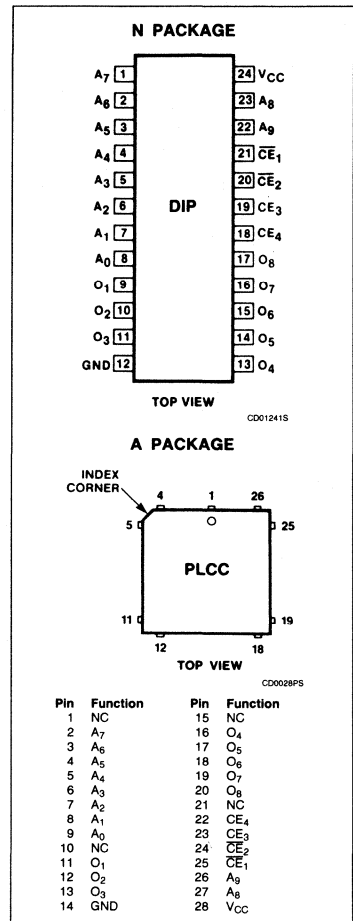
FEATURES

- Address access time: 30ns max
- Power dissipation: 76 μ W/bit typ
- Input loading: -100μ A max
- On-chip address decoding
- Four chip enable inputs
- Outputs: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



8K-Bit TTL Bipolar PROM (1024 × 8)

82S181C

ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82S181C N
Plastic Dual Inline 300mil wide 24-pin	N82S181C N3
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82S181C A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage² V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage² V _{OL} Low V _{OH} High	$\overline{CE}_{1,2}$ = Low, CE _{3,4} = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current¹ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current¹ I _{OZ} Hi-Z State I _{OS} Short circuit	$\overline{CE}_{1,2}$ = High, CE _{3,4} = Low, V _{OUT} = 5.5V $\overline{CE}_{1,2}$ = High, CE _{3,4} = Low, V _{OUT} = 0.5V $\overline{CE}_{1,2}$ = Low, CE _{3,4} = High, V _{OUT} = 0V High Stored	-15		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		125	175	mA
Capacitance C _{IN} Input C _{OUT} Output	$\overline{CE}_{1,2}$ = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

8K-Bit TTL Bipolar PROM (1024 × 8)

82S181C

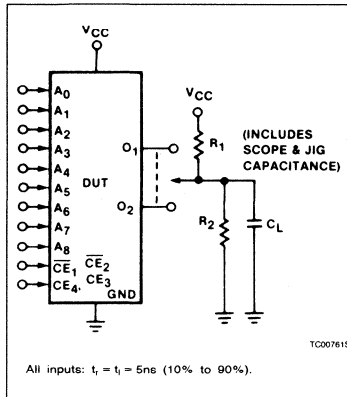
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access Time 4 T_{AA} T_{CE}	Output Output	Address Chip enable		25	30	ns
				15	20	
Disable time⁶ T_{CD}	Output	Chip disable		15	20	ns

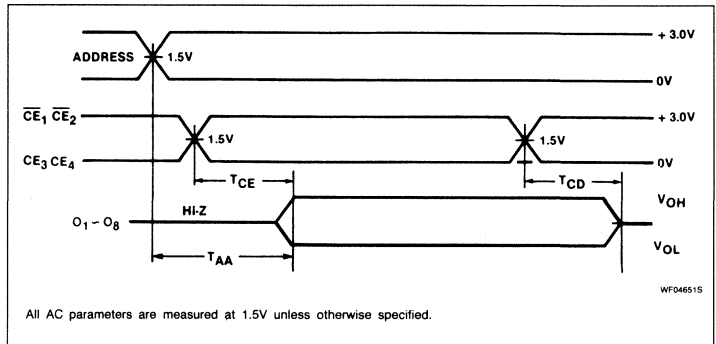
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82LS181 8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LS181 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82LS181 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

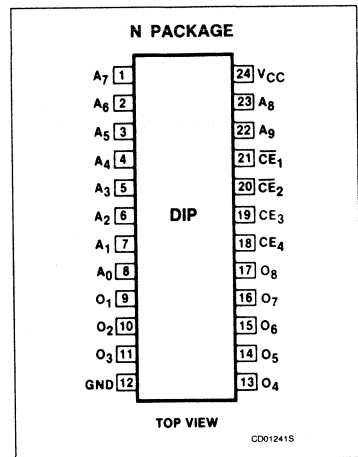
FEATURES

- Address access time: 120ns max
- Power dissipation: 37 μ W/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- Four chip enable inputs
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Outputs: Three-state

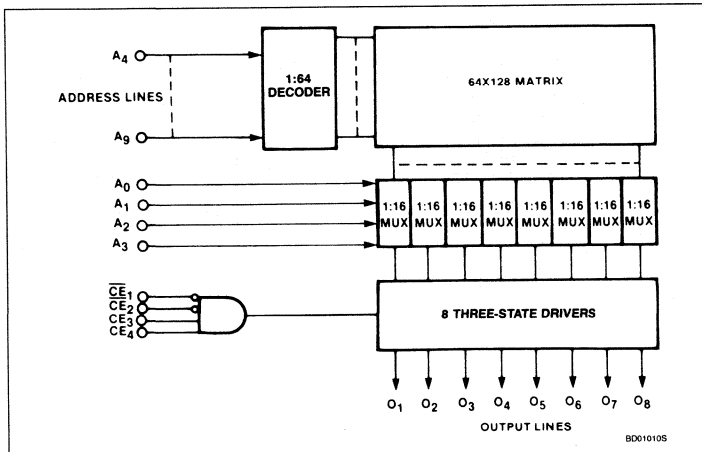
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (1024 × 8)

82LS181

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 600mil wide 24-pin	N82LS181 N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage² V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage² V _{OL} Low V _{OH} High	$\overline{CE}_{1,2}$ = Low, CE _{3,4} = High I _{OUT} = 4.8mA I _{OUT} = -1mA	2.4		0.45	V
Input current¹ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current¹ I _{OZ} Hi-Z State I _{OS} Short circuit ³	$\overline{CE}_{1,2}$ = High, CE _{3,4} = Low, V _{OUT} = 5.5V $\overline{CE}_{1,2}$ = High, CE _{3,4} = Low, V _{OUT} = 0.5V $\overline{CE}_{1,2}$ = Low, CE _{3,4} = High, V _{OUT} = 0V High Stored	-10		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		60	80	mA
Capacitance C _{IN} Input C _{OUT} Output	$\overline{CE}_{1,2}$ = High, CE _{3,4} = Low, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

8K-Bit TTL Bipolar PROM (1024 × 8)

82LS181

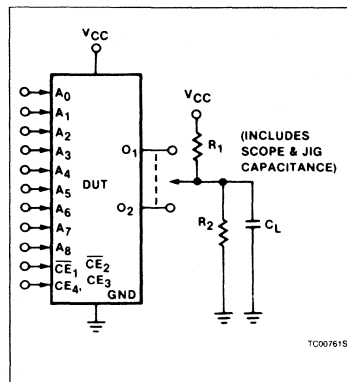
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address Chip Enable		100	120	ns
				35	50	
Disable time⁶ T_{CD}	Output	Chip disable		35	50	ns

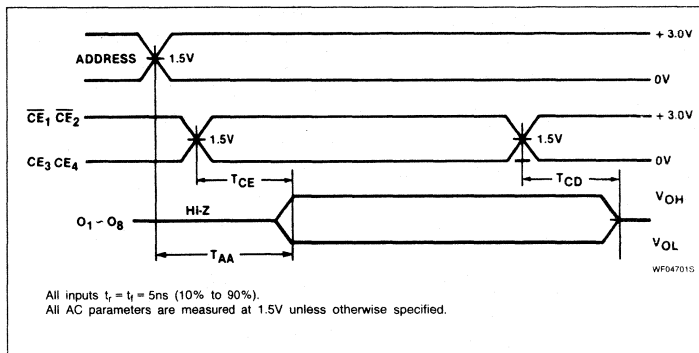
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of $1\mu\text{sec}$.
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S183 8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S183 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S183 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the output drivers are controlled solely by \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 lines.

A D-type latch is used to enable the Three-state output drivers. In the Latched Read mode, outputs are held in their previous state (High, Low, or High Z) as long as Strobe is Low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and caus-

es outputs to go to the High Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the High Z condition if the chip was disabled.

Ordering information can be found on the following page.

FEATURES

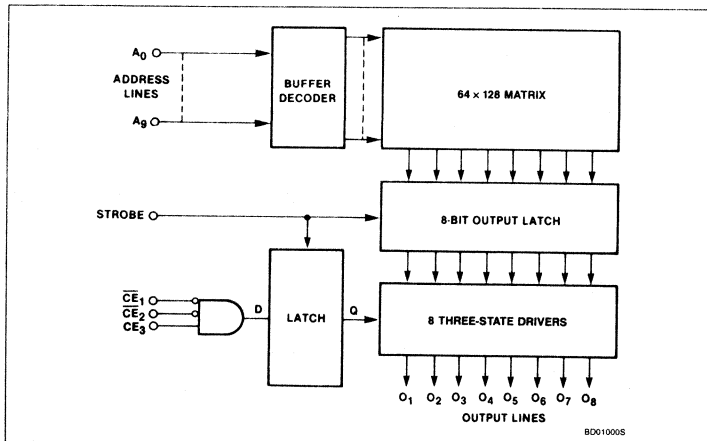
- Address access time: 60ns max
- Power dissipation: 80 μ W/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level

- Fully TTL compatible
- Three chip enable inputs
- Outputs: Three-state

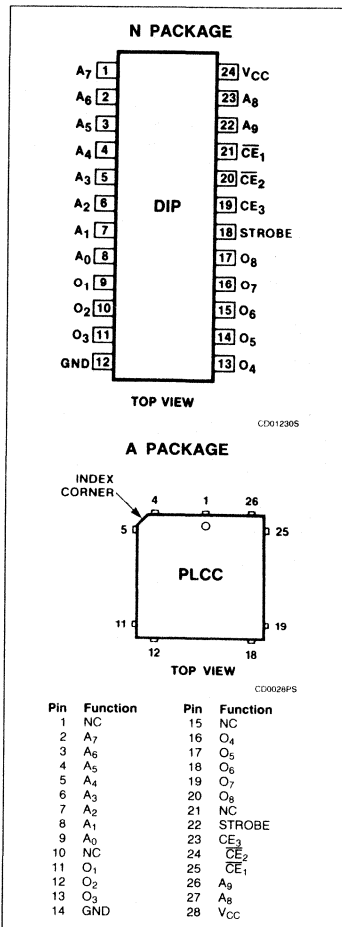
APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATION



8K-Bit TTL Bipolar PROM (1024 × 8)

82S183

DESCRIPTION	ORDER CODE
Plastic Dual Inline 600mil wide 24-pin	N82S183 N
Plastic Leaded chip carrier 450mil sq 28-pin	N82S183 A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} Supply voltage	+ 7	V_{dc}
V_{IN} Input voltage	+ 5.5	V_{dc}
T_A Operating T_{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS ⁴	LIMITS			UNIT
		Min	Typ ⁶	Max	
Input voltage V_{IL} Low V_{IH} High V_{IC} Clamp	$I_{IN} = -12\text{mA}$	2.0	-0.8	0.8 -1.2	V
Output voltage V_{OL} Low V_{OH} High	$\overline{CE}_{1,2} = \text{Low}$, $CE_3 = \text{Strobe} = \text{High}$ $I_{OUT} = 9.6\text{mA}$ $I_{OUT} = -2.0\text{mA}$	2.4		0.45	V
Input current⁴ I_{iL} Low I_{iH} High	$V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$	25		-100 25	μA
Output current⁴ I_{OZ} Hi-Z State I_{OS} Short circuit ¹	$\overline{CE} = \text{High}$ or $CE = \text{Low}$, $V_{OUT} = 5.5\text{V}$ $\overline{CE} = \text{High}$ or $CE = \text{Low}$, $V_{OUT} = 0.5\text{V}$ $\overline{CE} = \text{Low}$, $CE = \text{High}$, $V_{OUT} = 0\text{V}$, High stored	-15		40 -40 -70	μA mA
Supply current I_{CC}	$V_{CC} = 5.25\text{V}$		130	175	mA
Capacitance C_{IN} Input C_{OUT} Output	$\overline{CE}_{1,2} = \text{High}$ or $CE_3 = \text{Low}$, $V_{CC} = 5.0$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8		pF

8K-Bit TTL Bipolar PROM (1024 × 8)

82S183

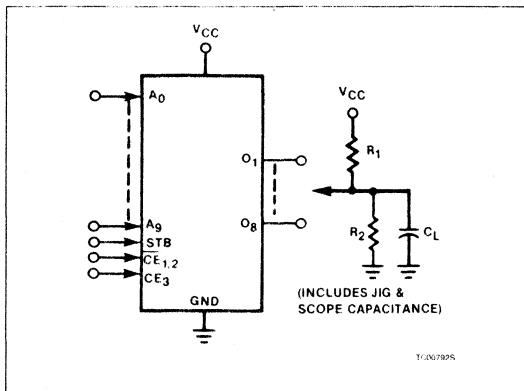
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	TEST CONDITIONS	Min	Typ ⁶	Max	UNIT
Access time² T_{AA} T_{CE}	Output Output	Address Chip enable	Latched or transparent read		45 25	60 40	ns
Disable time^{2,7} T_{CD}	Output	Chip disable			25	40	
Set-up and hold time³ T_{CDS} Set-up time T_{CDH} Hold time	Output	Chip enable	Latched read only	40 10			ns
T_{ADH} Hold time			Address	0			
Pulse width³ T_{SW} Strobe			Latched read only	30	15		ns
Latch time³ T_{SL} Strobe				60	35		ns
Delatch time^{3,7} T_{DL} Strobe						30	ns

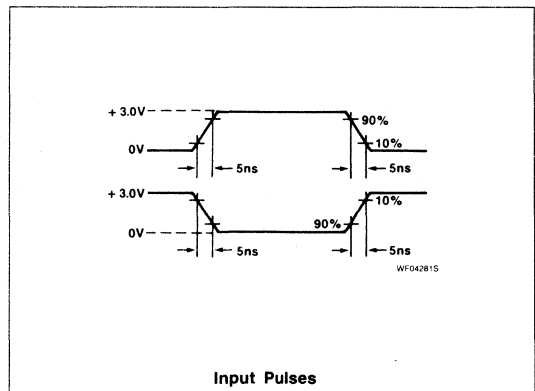
NOTES:

- No more than one output should be grounded at the same time and Strobe should be disabled. Strobe is in High state.
- If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed the T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or High impedance state after it has been enabled.
- In Latched Read Mode data from any selected address will be held on the output when Strobe is lowered. Only when Strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the output if the chip enable conditions enable the outputs.
- Positive current is defined as into the terminal referenced.
- Areas shown by crosshatch are latched data from previous address.
- Typical values are $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.
- All AC parameters are measured at 1.5V unless otherwise specified.

TEST LOAD CIRCUIT



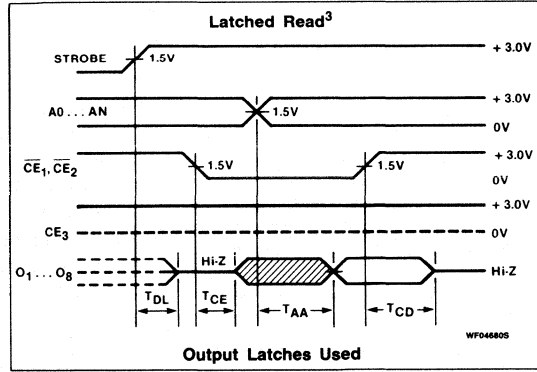
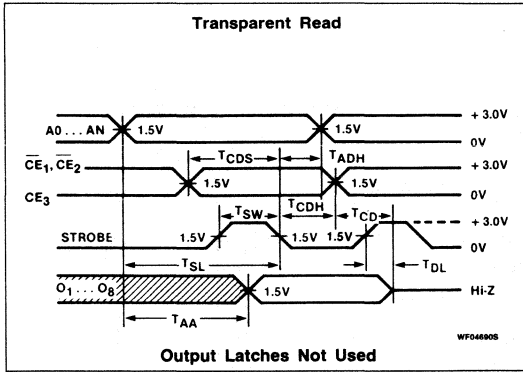
VOLTAGE WAVEFORM



8K-Bit TTL Bipolar PROM (1024 × 8)

82S183

TIMING DIAGRAMS⁸



82S185 8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

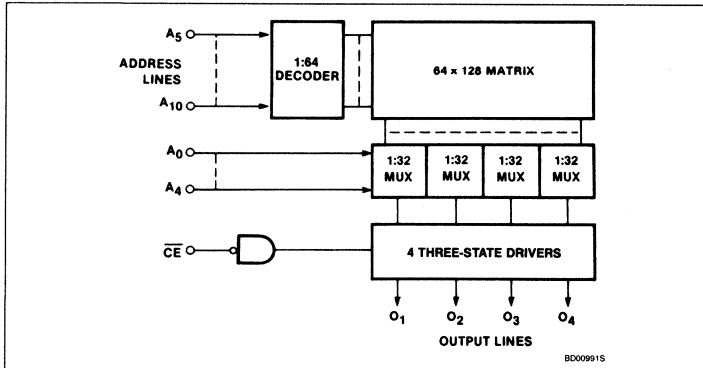
FEATURES

- Low power dissipation: 50 μ W/bit typ
- Address access time: 100ns max
- Input loading: -100 μ A max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One chip enable input
- Outputs: Three-state

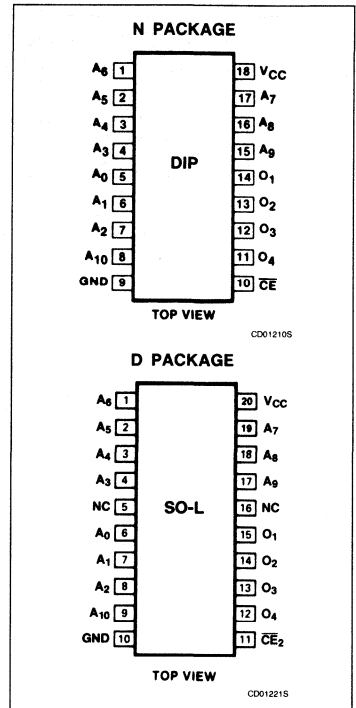
APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATION



8K-Bit TTL Bipolar PROM (2048 × 4)

82S185

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 18-pin	N82S185 N
Plastic Small Outline 300mil wide 20-pin	N82S185 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage¹ V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage¹ V _{OL} Low V _{OH} High	\overline{CE} = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current² I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{oz} Hi-Z State I _{os} Short circuit ³	\overline{CE} = High, V _{OUT} = 0.5V, \overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = Low, V _{OUT} = 0V High stored	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		90	120	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

8K-Bit TTL Bipolar PROM (2048 × 4)

82S185

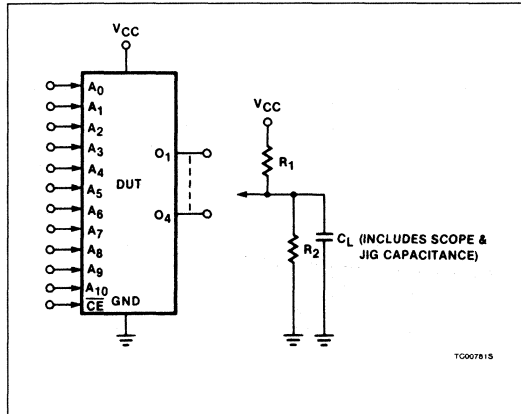
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time ⁴ T_{AA} T_{CE}	Output Output	Address Chip Enable		70	100	ns
				30	40	
Disable time ⁶ T_{CD}	Output	Chip disable		30	40	ns

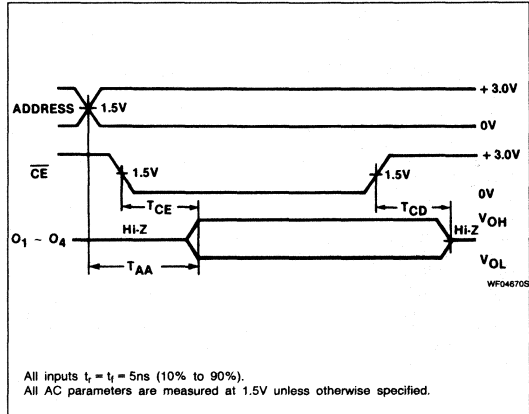
NOTES:

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of $1\mu\text{sec}$.
5. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5\text{ns}$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82S185A 82S185B 8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

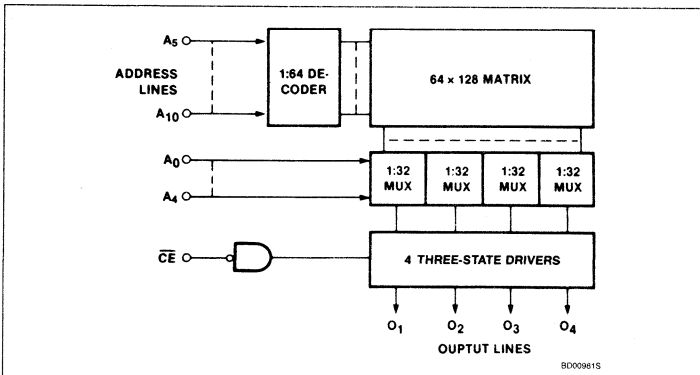
The 82S185A and 82S185B are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for memory expansion. It features Three-state outputs for optimization of word expansion in based organizations.

Ordering information can be found on the following page.

The 82S185A and 82S185B devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

BLOCK DIAGRAM



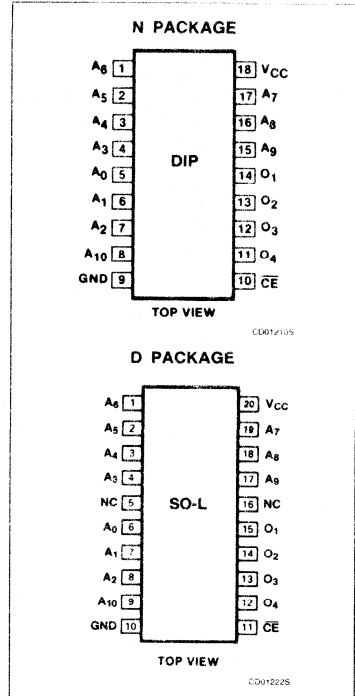
FEATURES

- Low power dissipation: 70 μ W/bit typ
- Address access time:
 - N82S185A: 50ns max
 - N82S185B: 45ns max
- Input loading: -100 μ A max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One chip enable input
- Outputs: Three-state

APPLICATIONS

- Microprogramming
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



8K-Bit TTL Bipolar PROM (2048 × 4)

82S185A, 82S185B

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 18-pin	N82S185A N • N82S185B N
Plastic Small Outline 300mil wide 20-pin	N82S185A D • N82S185B D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage					
V _{IL} Low	V _{CC} = 4.75V		0.8		V
V _{IH} High	V _{CC} = 5.25V	2.0			
V _{IC} Clamp	I _{IN} = -12mA		-0.8	-1.2	
Output voltage					
V _{OL} Low	\overline{CE} = Low I _{OUT} = 16mA			0.45	V
V _{OH} High	I _{OUT} = -2mA	2.4			
Input current					
I _{IL} Low	V _{IN} = 0.45V			-100	μA
I _{IH} High	V _{IN} = 5.5V			40	
Output current					
I _{OZ} Hi-Z State	\overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = High, V _{OUT} = 5.5V			-40 40	μA
I _{OS} Short circuit ³	\overline{CE} = Low, V _{OUT} = 0V High stored	-15		-70	mA
Supply current					
I _{CC}	V _{CC} = 5.25V		110	155	mA
Capacitance					
C _{IN} Input	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V		5		pF
C _{OUT} Output	V _{OUT} = 2.0V		8		

8K-Bit TTL Bipolar PROM (2048 × 4)

82S185A, 82S185B

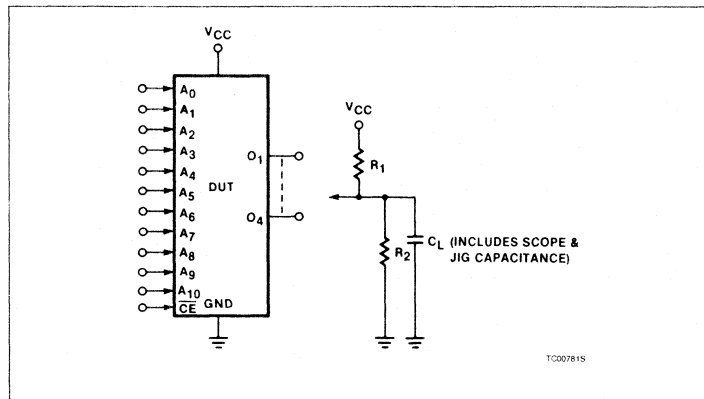
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	N82S185A			N82S185B			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
Access time ⁴ T_{AA} T_{CE}	Output	Address		40	50			45	ns
	Output	Chip Enable		20	30			25	
Disable time ⁶ T_{CD}	Output	Chip disable		20	30			25	ns

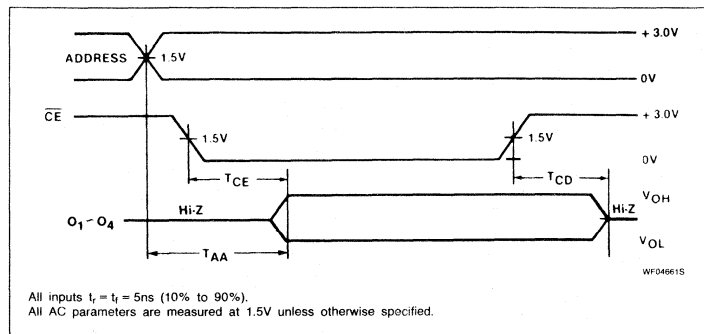
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_C = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82HS187 82HS187A 8K-Bit TTL Bipolar PROM

Product Specification

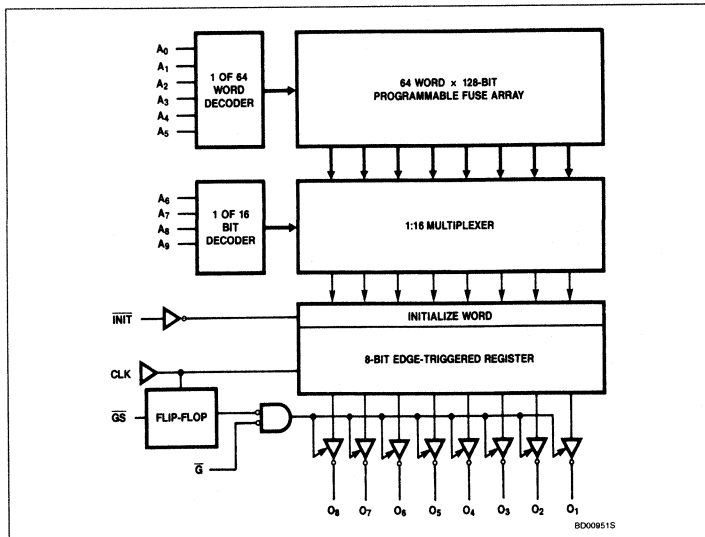
Bipolar Memory Products

DESCRIPTION

The 82HS187 is a programmable read only memory containing D-type, master-slave data registers. The 82HS187 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is Three-state for ease in connection to bus-organized systems. The combination of on-chip registers and Three-state outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition whenever the asynchronous chip enable (\bar{G}) is High. The outputs are enabled when (\bar{GS}) is brought Low before the rising edge of the clock and (\bar{G}) is held Low. The (\bar{GS}) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC} .

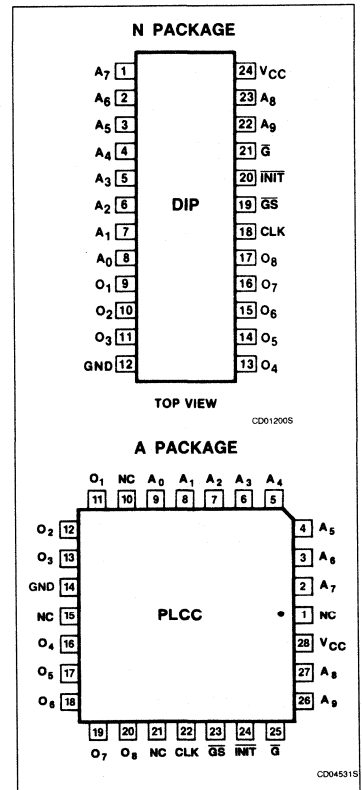
BLOCK DIAGRAM



The 82HS187 also features an initialize function, \bar{INIT} . The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on \bar{INIT} . The initialize function is asynchronous and is loaded into the output register and will appear at the outputs upon an application of a Low on \bar{INIT} if the outputs are enabled, and will control the state of the data registers independent of all other inputs. The unprogrammed state of \bar{INIT} is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9 . During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the addresses and synchronous chip enable can be removed and the output data will remain stable.

PIN CONFIGURATION



FEATURES

- On-chip edge-triggered registers
- Programmable register with asynchronous Initialize function
- 24-pin 300mil-wide DIP package
- Read cycle "Address setup plus clock to output delay"
 - N82HS187: 55ns max
 - N82HS187A: 45ns max
- Outputs: Three-state
- Unprogrammed outputs are High level
- Synchronous and asynchronous enables for word expansion

8K-Bit TTL Bipolar PROM (1024 × 8)

82HS187/82HS187A

ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual-In-Line 300mil-wide 24-pin	N82HS187 N • N82HS187A N
Plastic Leaded Chip Carrier 450mil-sq 28-pin	N82HS187 A • N82HS187A A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{DC}
V _{IN} Input voltage	+5.5	V _{DC}
V _O Output voltage Off-state	+5.5	V _{DC}
T _A Operating	0 to +75	0°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage² V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage² V _{OL} Low V _{OH} High	\bar{G} , \bar{GS} = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.5	V
Input current¹ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.25V			-250 40	μA
Output current¹ I _{OZ} Hi-Z State I _{OS} Short circuit ³	\bar{G} = High, V _{OUT} = 5.25V \bar{G} = High, V _{OUT} = 0.5V \bar{G} , \bar{GS} = Low, V _{OUT} = 0V High Stored	-15		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		125	175	mA
Capacitance C _{IN} Input C _{OUT} Output	\bar{G} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

8K-Bit TTL Bipolar PROM (1024 × 8)

82HS187/82HS187A

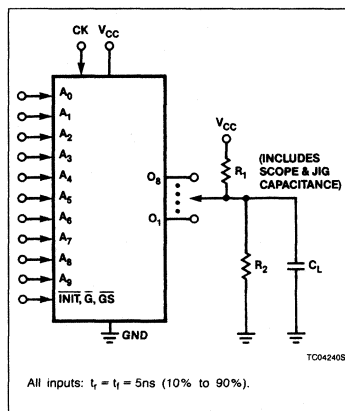
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER ⁴	TO	FROM	N82HS187			N82HS187A			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
t_{CSA} Setup	CK	Address	35			30			ns
t_{CHA} Hold			0			0			
t_{OC} Delay	Output	CK			20	0		15	ns
t_{WC} Width	H & L	CK	20	10		15	10		ns
t_{CSGS} Setup	CK	\overline{GS}	15			10			ns
t_{CHGS} Hold			5			5			
t_{OIN} Delay	Output	\overline{INIT}		12	30			25	ns
t_{OIN} Recovery	CK	\overline{INIT}	20	9		15			ns
t_{WIN} Width		\overline{INIT}	25			20			ns
t_{OG} Delay	Output	\overline{G}		11	25			20	ns
t_{OZC} ⁶ Delay	Output	CK		16	25			20	ns
t_{OZC} ⁶ Delay	Output	\overline{G}		14	25			20	ns

NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ s.
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

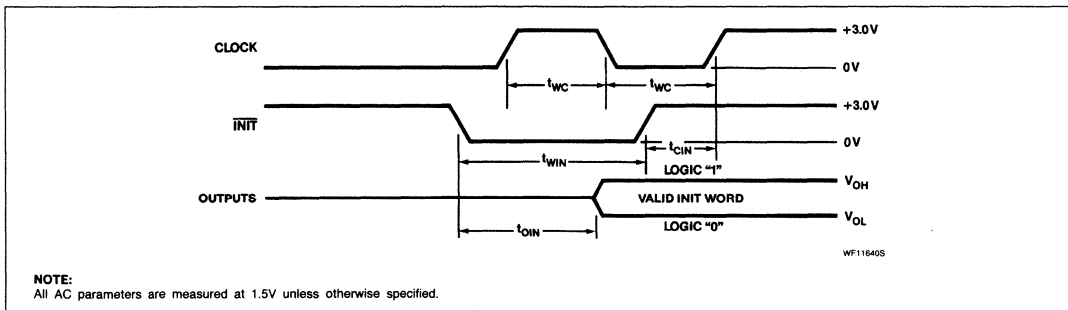
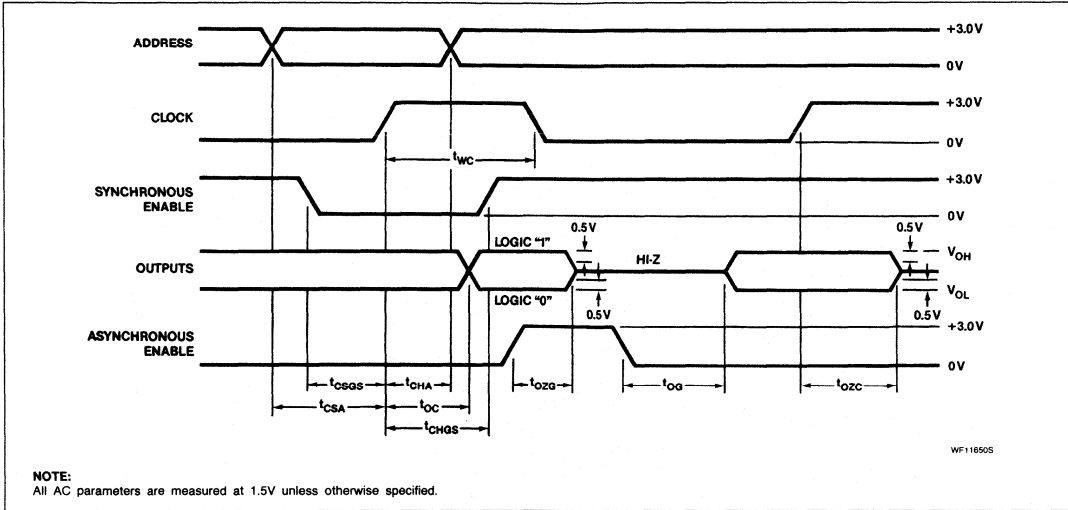
TEST LOAD CIRCUIT



8K-Bit TTL Bipolar PROM (1024 × 8)

82HS187/82HS187A

VOLTAGE WAVEFORMS



82HS189 82HS189A 8K-Bit TTL Bipolar PROM

Product Specification

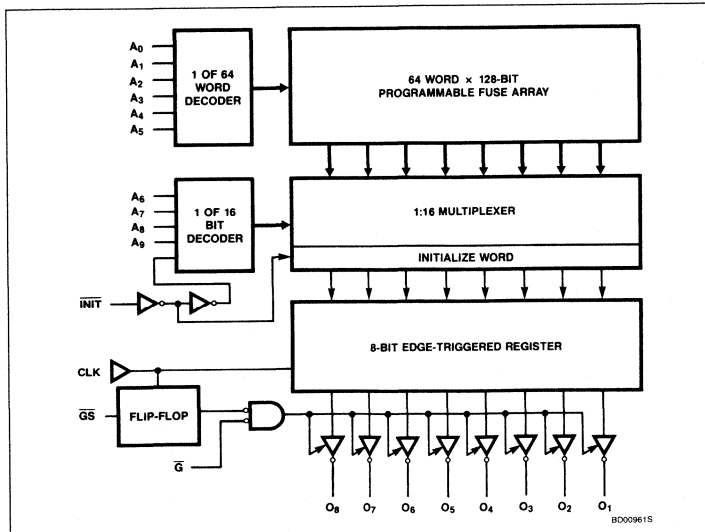
Bipolar Memory Products

DESCRIPTION

The 82HS189 is a programmable read only memory containing D-type, master-slave data registers. The 82HS189 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is Three-state for ease in connection to bus-organized systems. The combination of on-chip registers and Three-state outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition if the asynchronous chip enable (\bar{G}) is held High. The outputs are enabled when (\bar{GS}) is brought Low before the rising edge of the clock and (\bar{G}) is held Low. The (\bar{GS}) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC} .

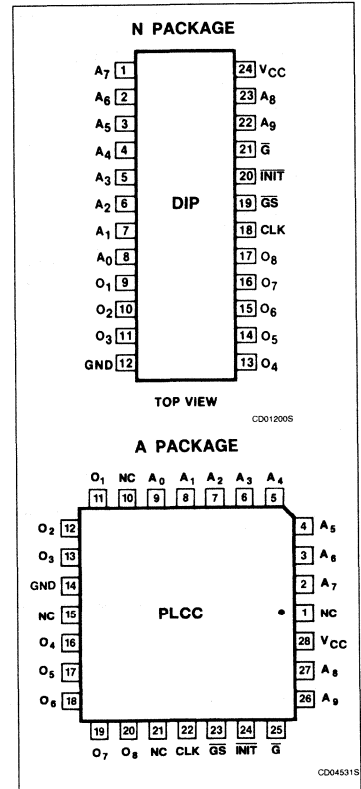
BLOCK DIAGRAM



The 82HS189 also features an initialize function, \bar{INIT} . The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on \bar{INIT} . The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of \bar{INIT} is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9 . During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the addresses and synchronous chip enable can be removed and the output data will remain stable.

PIN CONFIGURATION



FEATURES

- On-chip edge-triggered registers
- Asynchronous and synchronous enables for word expansion
- Programmable register with synchronous initialize function
- 24-pin 300mil package
- Read cycle "Address Setup plus Clock to Output Delay"
 - 82HS189: 55ns max
 - 82HS189A: 45ns max
- Unprogrammed outputs are High level
- Outputs: Three-state

8K-Bit TTL Bipolar PROM (1024 × 8)

82HS189/82HS189A

ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual-In-Line 300mil-wide 24-pin	N82HS189 N • N82HS189A N
Plastic Leaded Chip Carrier 450mil-sq 28-pin	N82HS189 A • N82HS189A A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{DC}
V _{IN} Input voltage	+5.5	V _{DC}
V _O Output voltage Off-state	+5.5	V _{DC}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage² V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage² V _{OL} Low V _{OH} High	$\bar{G}, \bar{GS} = \text{Low}$ I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.5	V
Input current¹ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.25V			-250 40	μA
Output current¹ I _{OZ} Hi-Z State I _{OS} Short circuit ³	$\bar{G} = \text{High}, V_{\text{OUT}} = 5.25\text{V}$ $\bar{G} = \text{High}, V_{\text{OUT}} = 0.5\text{V}$ $\bar{G}, \bar{GS} = \text{Low}, V_{\text{OUT}} = 0\text{V}$ High Stored	-15		40 -40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		125	175	mA
Capacitance C _{IN} Input C _{OUT} Output	$\bar{G} = \text{High}, V_{\text{CC}} = 5.0\text{V}$ V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

8K-Bit TTL Bipolar PROM (1024 × 8)

82HS189/82HS189A

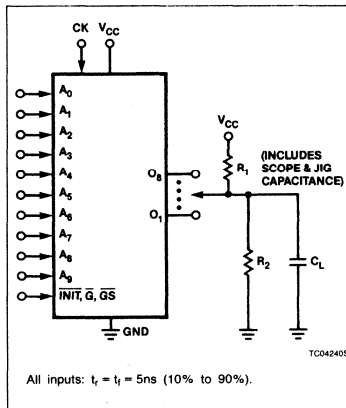
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq 75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER ⁴	TO	FROM	N82HS189			N82HS189A			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
t _{CSA} Setup t _{CHA} Hold	CK	Address	35 0			30 0			ns
t _{OC} Delay	Output	CK		10	20	0		15	ns
t _{wC} Width	H & L	CK	20	10		15			ns
t _{CSGS} Setup t _{CHGS} Hold	CK	$\overline{\text{GS}}$	15 5			10 5			ns
t _{CSIN} Setup t _{CHIN} Hold	CK	$\overline{\text{INIT}}$	25 0	8		20 0			ns
t _{OG} Delay	Output	$\overline{\text{G}}$		11	25			20	ns
t _{OZC} ⁶ Delay	Output	CK		16	25			20	ns
t _{OZG} ⁶ Delay	Output	$\overline{\text{G}}$		14	25			20	ns

NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μs .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

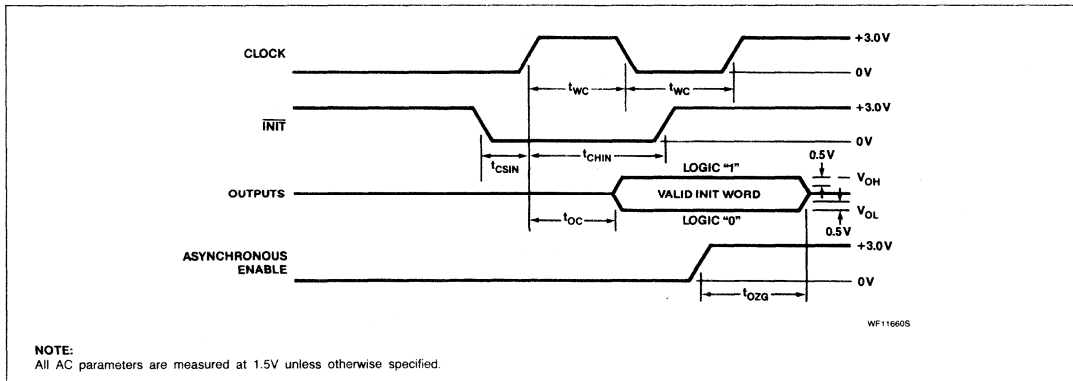
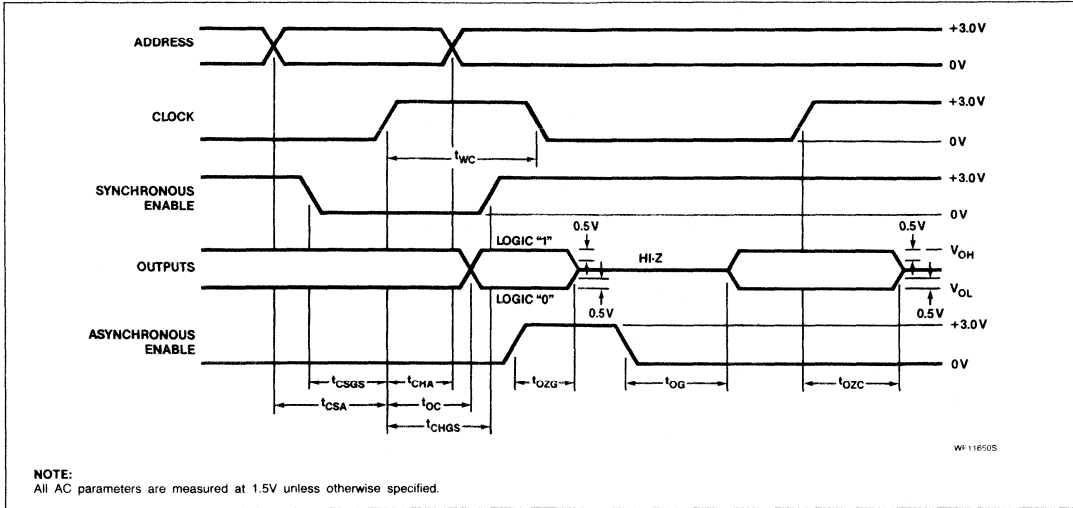
TEST LOAD CIRCUIT



8K-Bit TTL Bipolar PROM (1024 × 8)

82HS189/82HS189A

VOLTAGE WAVEFORMS



16-bit TTL Bipolar PROM

82S191/82S191A	16,384-bit PROM (2048 x 8)273
82S191C	16,384-bit PROM (2048 x 8)276
82HS195/82HS195A/ 82HS195B	16,384-bit PROM (4096 x 4)279

82S191 82S191A 16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S191 and 82S191A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191 and 82S191A are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191 and 82S191A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

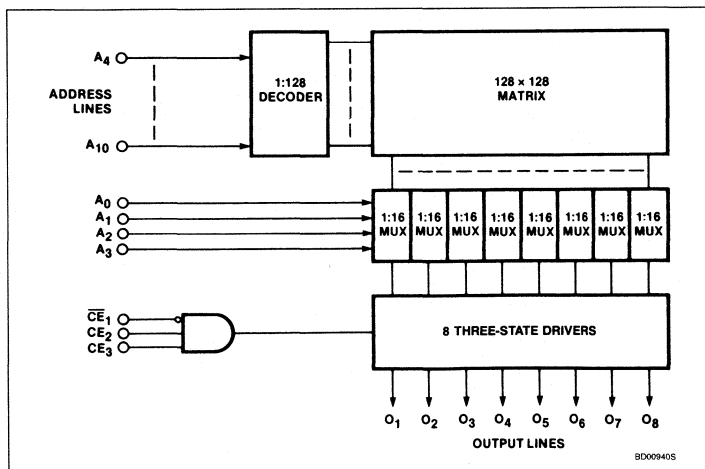
FEATURES

- **Address access time:**
 - N82S191: 80ns max
 - N82S191A: 55ns max
- **Power dissipation: 40μW/bit typ**
- **Input loading: -100μA max**
- **Three chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Outputs: Three-state**

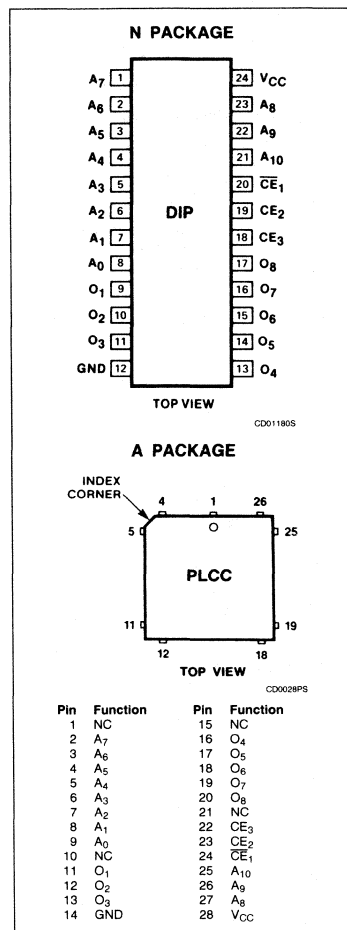
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM



PIN CONFIGURATION



16K-Bit TTL Bipolar PROM (2048 × 8)

82S191, 82S191A

ORDERING CODE

PACKAGE DESCRIPTION	ORDER CODE
Plastic Dual Inline 600mil wide 24-pin	N82S191 N • N82S191A N
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82S191 A • N82S191A A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ₅	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE}_1 = Low, CE _{2,3} = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current¹ I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current¹ I _{OZ} Hi-Z state I _{OS} Short circuit ³	\overline{CE}_1 = High, CE _{2,3} = Low, V _{OUT} = 0.5 \overline{CE}_1 = High, CE _{2,3} = Low, V _{OUT} = 5.5 \overline{CE}_1 = Low, CE _{2,3} = High, V _{OUT} = 0V	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		130	175	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE}_1 = High, CE _{2,3} = Low, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

16K-Bit TTL Bipolar PROM (2048 × 8)

82S191, 82S191A

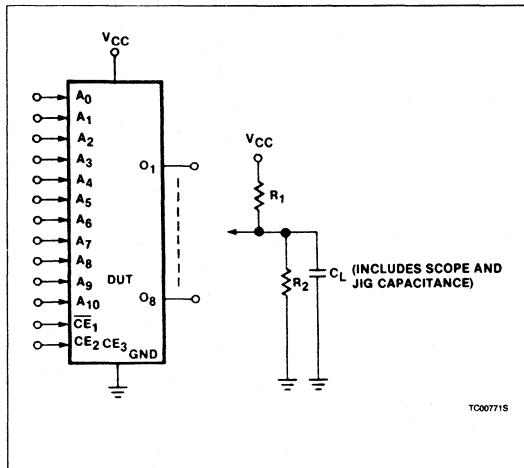
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S191			N82S191A			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address Chip enable		50 30	80 40		50 20	55 30	ns
Disable time⁶ T_{CD}	Output	Chip disable		30	40		20	30	ns

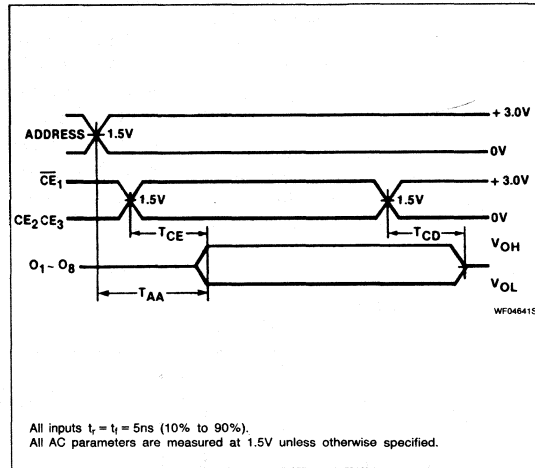
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S191C 16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

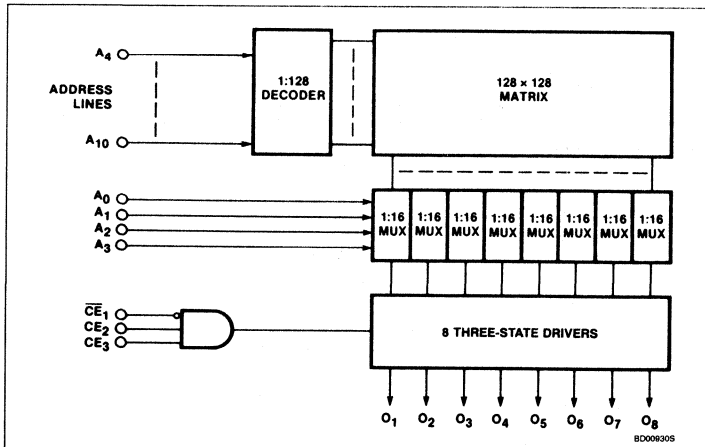
The 82S191C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191C is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191C devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

BLOCK DIAGRAM



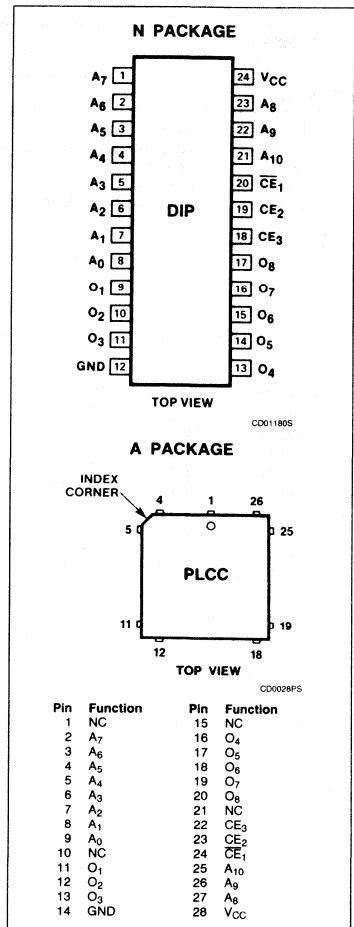
FEATURES

- Address access time: 35ns max
- Power dissipation: 40 μ W/bit typ
- Input loading: -100 μ A max
- Three chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Outputs: Three-state

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



16K-Bit TTL Bipolar PROM (2048 × 8)

82S191C

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 600mil wide 24-pin	N82S191C N
Plastic Dual Inline 300mil wide 24-pin	N82S191C N3
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82S191C A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} Supply voltage	+7	V_{dc}
V_{IN} Input voltage	+5.5	V_{dc}
V_O Output voltage Off-state	+5.5	V_{dc}
T_A Temperature range Operating	0 to +75	°C
T_{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V_{IL} Low V_{IH} High V_{IC} Clamp	$I_{IN} = -12\text{mA}$	2.0	-0.8	0.8 -1.2	V
Output voltage V_{OL} Low V_{OH} High	$\overline{CE}_1 = \text{Low}, CE_{2,3} = \text{High}$ $I_{OUT} = 9.6\text{mA}$ $I_{OUT} = -2\text{mA}$	2.4		0.45	V
Input current I_{IL} Low I_{IH} High	$V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-100 40	μA
Output current I_{OZ} Hi-Z state I_{OS} Short circuit ³	$\overline{CE}_1 = \text{High}, CE_{2,3} = \text{Low},$ $V_{OUT} = 0.5$ $\overline{CE}_1 = \text{High}, CE_{2,3} = \text{Low},$ $V_{OUT} = 5.5$ $\overline{CE}_1 = \text{Low}, CE_{2,3} = \text{High},$ $V_{OUT} = 0\text{V}$			-40 40 -70	μA mA
Supply current I_{CC}	$V_{CC} = 5.25\text{V}$		130	175	mA
Capacitance C_{IN} Input C_{OUT} Output	$V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8		pF

16K-Bit TTL Bipolar PROM (2048 × 8)

82S191C

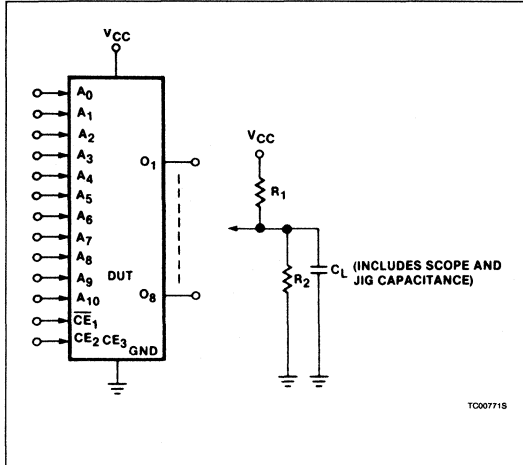
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output Output	Address Chip enable		30 15	35 20	ns
Disable time⁶ T_{CD}	Output	Chip disable		15	20	ns

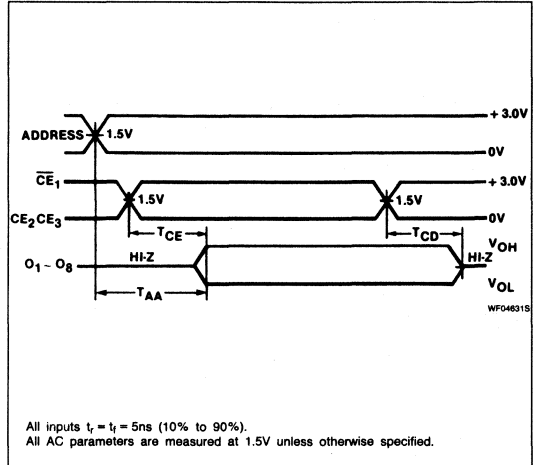
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82HS195 82HS195A 82HS195B 16K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS195 is field programmable, which means that custom patterns are immediately available by following the Generic II fusing procedure. The Signetics 82HS195 is supplied with all outputs at logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

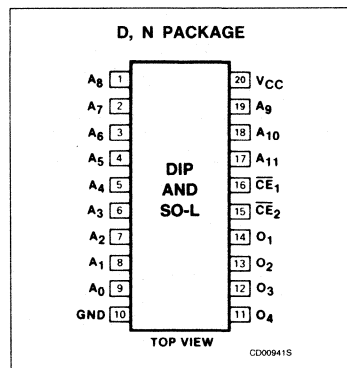
Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

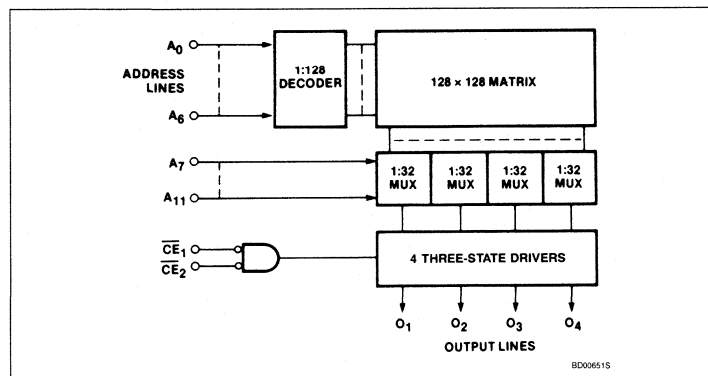
FEATURES

- Low power dissipation: 35μ W/bit typ
- Address access time:
 - N82HS195: 45ns max
 - N82HS195A: 35ns max
 - N82HS195B: 25ns max
- Input loading: 100μ A max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: Three-state
- 2 chip enable inputs

PIN CONFIGURATION



BLOCK DIAGRAM



16K-Bit TTL Bipolar PROM (4096 × 4)

82HS195, 82HS195A, 82HS195B

ORDERING CODE

PACKAGE DESCRIPTION	ORDER CODES
Plastic Dual Inline 300mil wide 20-pin	N82HS195 N • N82HS195A N • N82HS195B N
Plastic Small Outline 300mil wide 20-pin	N82HS195 D • N82HS195A D • N82HS195B D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low ³ V _{IH} High ³ V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE}_1 & \overline{CE}_2 = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ⁴	\overline{CE}_1 & \overline{CE}_2 = High, V _{OUT} = 0.5V \overline{CE}_1 & \overline{CE}_2 = High, V _{OUT} = 5.5V \overline{CE}_1 & \overline{CE}_2 = Low, V _{OUT} = 0V High Stored	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		120	145	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE}_1 & \overline{CE}_2 = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

16K-Bit TTL Bipolar PROM (4096 × 4)

82HS195, 82HS195A, 82HS195B

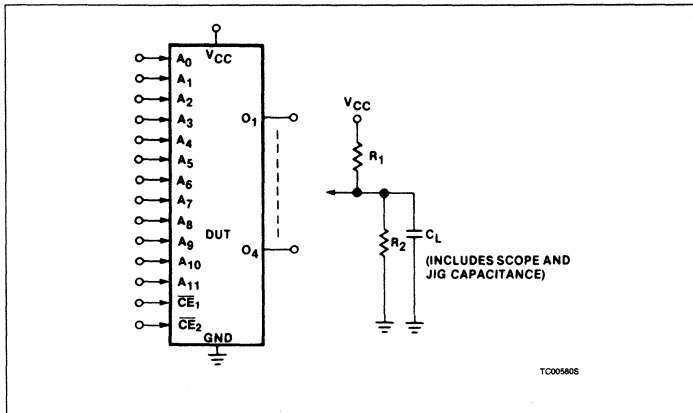
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82HS195			N82HS195A			N82HS195B			UNIT
			Min	Typ ⁵	Max	Min	Typ ⁵	Max	Min	Typ ⁵	Max	
Access Time ⁷ T_{AA} T_{CE}	Output	Address		35	45		25	35		20	25	ns
		Chip Enable		20	25		15	20		10	15	
		Output										
Disable time ⁶ T_{CD}	Output	Chip disable		20	25		15	20		10	15	ns
		Output										

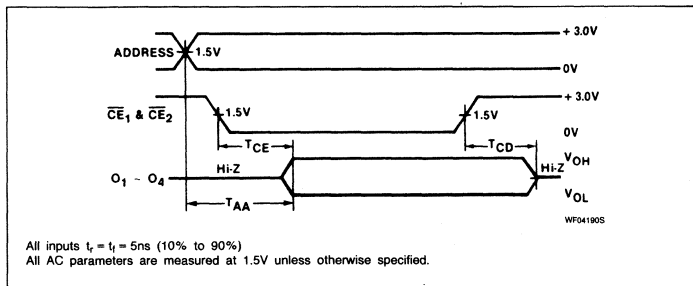
NOTES:

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of the short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of 1 μ sec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



32K-bit TTL Bipolar PROM

82S321	32,768-bit PROM (4096 x 8)285
82HS321/82HS321A/ 82HS321B	32,768-bit PROM (4096 x 8)288

82S321 32K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S321 is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

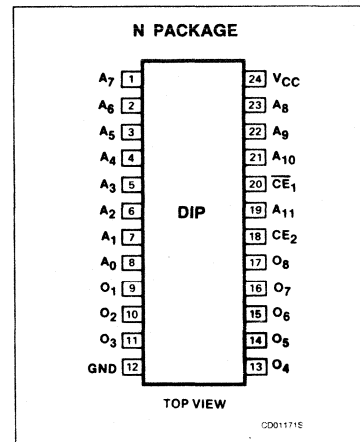
FEATURES

- Address access time: 70ns max
- Power dissipation: 20 μ W/bit typ
- Input loading: -100 μ A max
- Two chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Outputs: Three-state

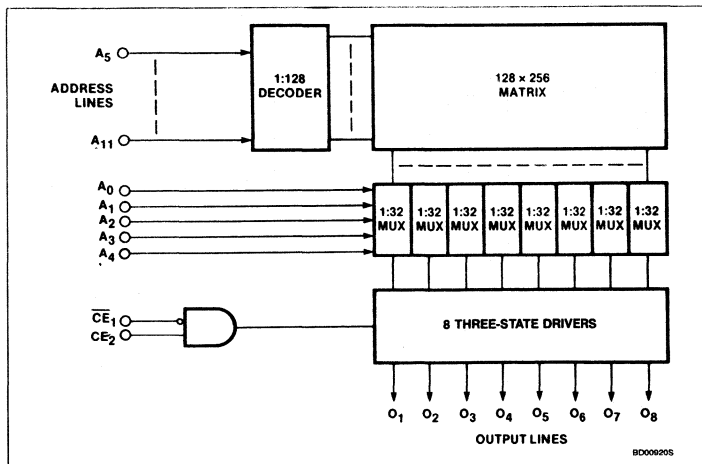
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



32K-Bit TTL Bipolar PROM (4096 × 8)

82S321

ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82S321 N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	CE ₁ = Low, CE ₂ = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ³	CE ₁ = High, CE ₂ = Low, V _{OUT} = 0.5 CE ₁ = High, CE ₂ = Low, V _{OUT} = 5.5 CE ₁ = Low, CE ₂ = High, V _{OUT} = 0V	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25		130	175	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

32K-Bit TTL Bipolar PROM (4096 × 8)

82S321

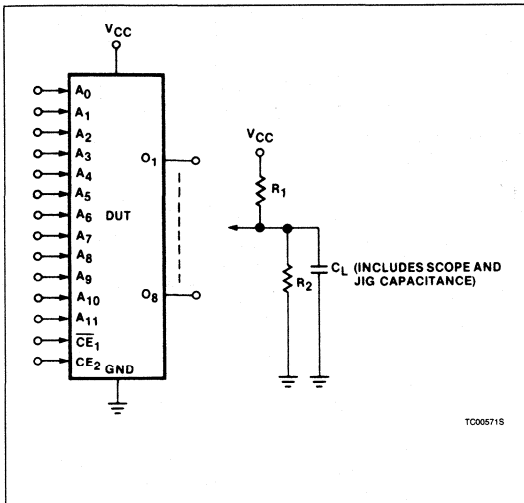
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time ⁴ T_{AA} T_{CE}	Output Output	Address		60	70	ns
		Chip enable		20	25	
Disable time ⁶ T_{CD}	Output	Chip disable		20	25	ns

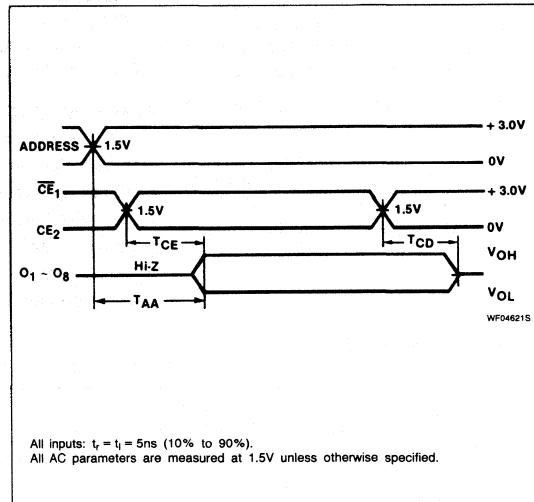
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82HS321 82HS321A 82HS321B 32K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

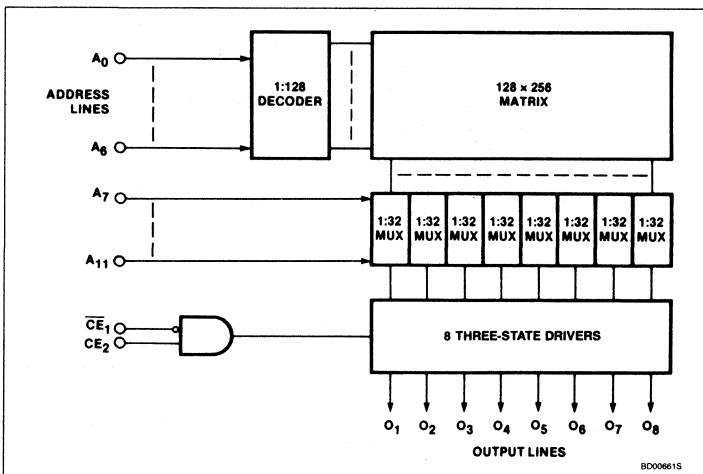
FEATURES

- Address access time:
N82HS321: 45ns max
N82HS321A: 35ns max
N82HS321B 30ns max
- Power dissipation: 20 μ W/bit typ
- Input loading: -100 μ A max
- 2 chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: Three-state

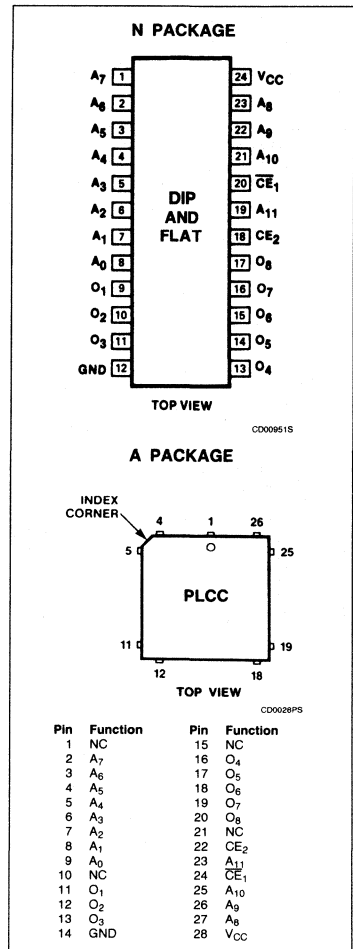
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATION



32K-Bit TTL Bipolar PROM (4096 × 8)

82HS321, 82HS321A, 82HS321B

ORDERING CODE

PACKAGE DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82HS321 N • N82HS321A N • N82HS321B N
Ceramic Dual Inline 600mil wide 24-pin	N82HS321 F • N82HS321A F • N82HS321B F
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82HS321 A • N82HS321A A • N82HS321B A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low ³ V _{IH} High ³ V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE}_1 = Low, CE ₂ = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z state I _{OS} Short circuit ⁴	\overline{CE}_1 = High, CE ₂ = Low, V _{OUT} = 0.5 \overline{CE}_1 = High, CE ₂ = Low, V _{OUT} = 5.5 \overline{CE}_1 = Low, CE ₂ = High, V _{OUT} = 0V	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		130	175	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE}_1 = High, CE ₂ = Low, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

32K-Bit TTL Bipolar PROM (4096 × 8)

82HS321, 82HS321A, 82HS321B

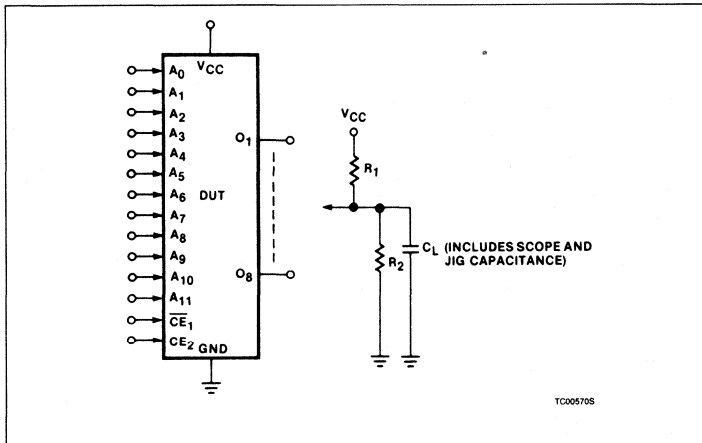
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82HS321			N82HS321A			N82HS321B			UNIT
			Min	Typ ⁵	Max	Min	Typ ⁵	Max	Min	Typ ⁵	Max	
Access time ⁷ T_{AA} T_{CE}	Output	Address		40	45		30	35		25	30	ns
		Chip enable		25	30		20	25		18	20	
		Chip disable		25	30		20	25		18	20	
Disable time ⁶ T_{CD}	Output	Chip disable		25	30		20	25		18	20	ns

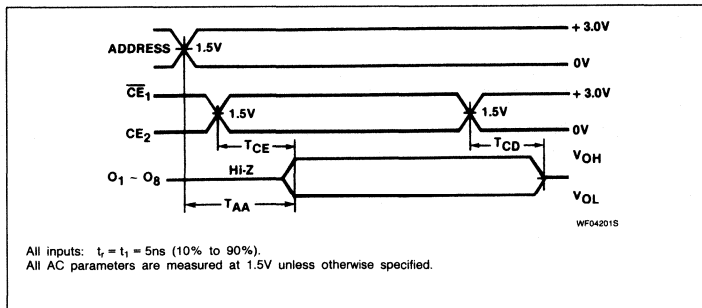
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of 1 μ sec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



64K-bit TTL Bipolar PROM

82HS641/82HS641A/

82HS641B

65,536-bit PROM (8192 x 8) 293

82HS641 82HS641A 82HS641B 64K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

The 82HS641 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing Procedure. The 82HS641 is supplied with all outputs at a logical High. Outputs are programmed to a logic low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 1 chip enable input for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused applications.

Ordering information can be found on the following page.

This device is also processed to military requirements for operating over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

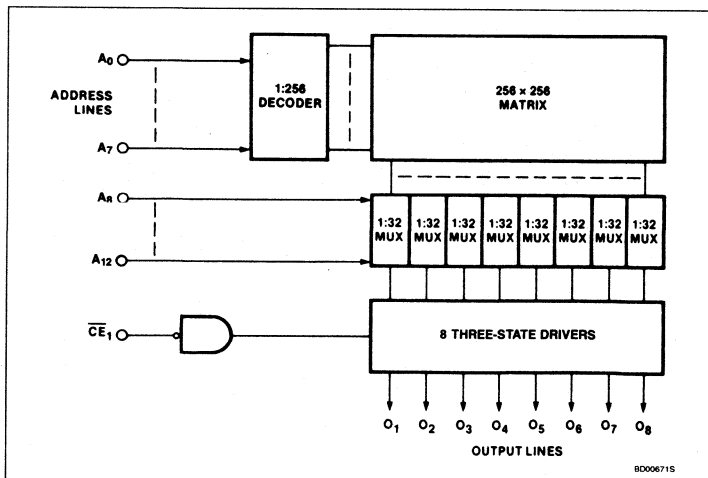
FEATURES

- Address access time:
 - N82HS641 55ns max
 - N82HS641A 45ns max
 - N82HS641B 35ns max
- Power dissipation: 10μW/bit typ
- Input loading: -100μA max
- One chip enable input
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: Three-state

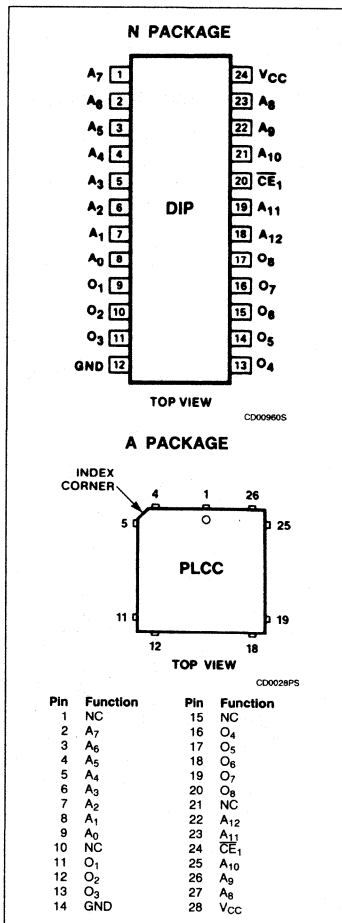
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATION



64K-Bit TTL Bipolar PROM (8192 × 8)

82HS641, 82HS641A, 82HS641B

ORDERING CODE

PACKAGE DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82HS641 N • N82HS641A N • N82HS641B N
Ceramic Dual Inline 600mil wide 24-pin	N82HS641 F • N82HS641A F • N82HS641B F
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82HS641 A • N82HS641A A • N82HS641B A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low ³ V _{IH} High ³ V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE}_1 = Low I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ⁴	\overline{CE}_1 = High, V _{OUT} = 0.5V \overline{CE}_1 = High, V _{OUT} = 5.5V \overline{CE}_1 = Low, V _{OUT} = 0V	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		130	175	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE}_1 = High V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

64K-Bit TTL Bipolar PROM (8192 × 8)

82HS641, 82HS641A, 82HS641B

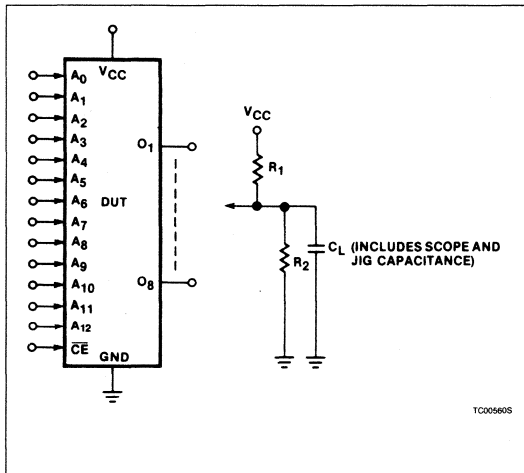
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82HS641			N82HS641A			N82HS641B			UNIT
			Min	Typ ⁵	Max	Min	Typ ⁵	Max	Min	Typ ⁵	Max	
Access time ⁷ T_{AA} T_{CE}	Output	Address		50	55		40	45		30	35	ns
			Output	Chip enable	30	35		20	25		15	
	Disable time ⁶ T_{CD}	Output	Chip disable		30	35		20	25		15	20

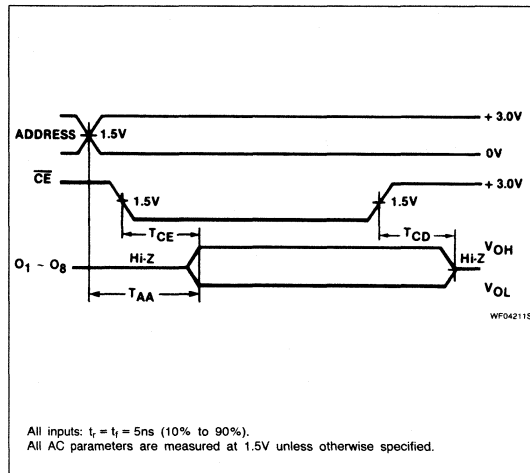
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



ECL MEMORIES

ECL RAM	299
---------------	-----

Bipolar ECL RAM

10422B	256 x 4-bit RAM.301
10422C	256 x 4-bit RAM.304
10470A	4096 x 1-bit RAM.307
100422B	256 x 4-bit RAM.310
100422C	256 x 4-bit RAM.313
100470A	4096 x 1-bit RAM.316
100474A	1024 x 4-bit RAM.319

10422B 1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10422B device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratchpad, control, and buffer storage applications. The 10422B is available in a slimline 24-pin dual-in-line, flat or leadless package. This circuit may be reconfigured as 512×2 or 1024×1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The Open Emitter outputs have a 50Ω drive capability. The input pull-down resistor to V_{CC} is $50,000\Omega$ typical for the block selects.

Ordering information can be found on the following page.

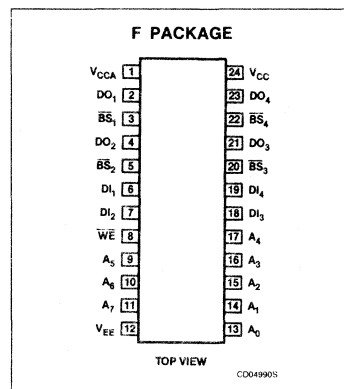
FEATURES

- 256 words \times 4 bits organization
- Fully compatible with 10K series ECL families
- Address access time:
- 10422B, 10ns max.
- Low power dissipation of 0.8mW/bit
- Operating temperature:
0°C to +75°C (ambient)
- Block select allows variable organization

APPLICATIONS

- High-speed scratchpad
- Control and buffer storage

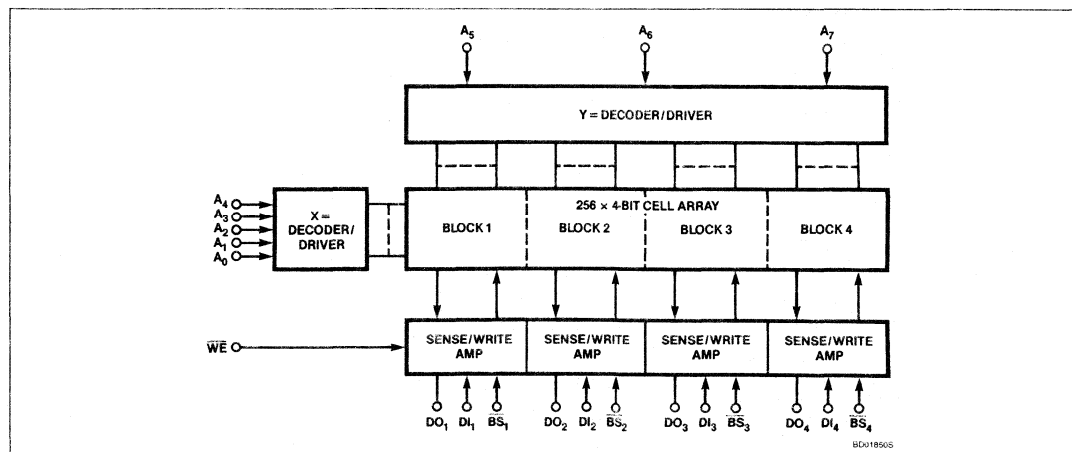
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{EE} Supply voltage	+0.5 to -7	V_{DC}
V_{IN} Input voltage	0 to V_{EE}	
I_O Output current	-30	mA
T_A Operating ambient temperature	0 to +75	°C
T_J Operating junction temperature	+125	
T_{STG} Storage temperature	-55 to +150	

BLOCK DIAGRAM



1K-Bit ECL Bipolar RAM (256 × 4)

10422B

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual-In-line 400mil wide 24-pin	10422B F

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
		Min	Max	Min	Max	Min	Max	
Input voltage								
V_{IH} High		-1.145	-0.840	-1.105	-0.810	-1.045	-0.720	V
V_{IL} Low		-1.870	-1.490	-1.850	-1.475	-1.830	-1.450	
Output voltage								
V_{OH} High	$V_{IH} = \text{Max}$	-1.0	-0.840	-0.960	-0.810	-0.900	-0.720	V
V_{OL} Low	$V_{IL} = \text{Min}$	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	
V_{OHT} Threshold HIGH	$V_{IH} = \text{Min}$	-1.020		-0.980		-0.920		
V_{OLT} Threshold LOW	$V_{IL} = \text{Max}$		-1.645		-1.630		-1.605	
Input current								
I_{IH} High	$V_{IH} = \text{Max}$		220		220		220	μA
I_{IL} Low	$V_{IL} = \text{Min}$	-50		-50		-50		
I_{IL} BS	$V_{IL} = \text{Min}$	0.5		0.5		0.5		
I_{EE} Supply current	$V_{IL} = \text{Min}$		200		200		200	mA

NOTES:

1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{AA}	Address access time			10	ns
t_{RBS}	Block select recovery time			5	
t_{ABS}	Block select access time			5	
t_{WD}	Write disable time			5	
t_{WPW}	Write pulse width	7			
t_{WR}	Write recovery time		4.5	9	
t_{WHA}	Address hold time	2	1		
t_{WHBS}	Block select hold time	2	1		
t_{WHD}	Data hold time	2	1		
t_{WSA}	Address setup time	3	1		
t_{WSBS}	Block select setup time	2	1		
t_{WSD}	Data setup time	2	1		
t_f	Output fall time		2		
t_r	Output rise time		2		
Capacitance					pF
C_{IN}	Input			8	
C_{OUT}	Output			8	

NOTES:

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

1K-Bit ECL Bipolar RAM (256 × 4)

10422B

TRUTH TABLE

MODE	INPUTS			OUTPUTS
	\overline{BS}_N	WE	DI_N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:

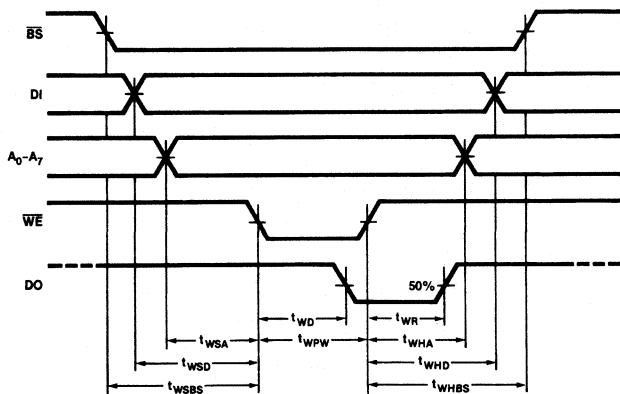
H = HIGH voltage level

L = LOW voltage level

X = Don't Care

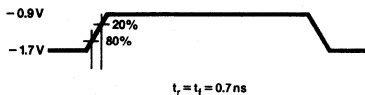
N = Blocks 1 - 4

TIMING DIAGRAMS



WF121805

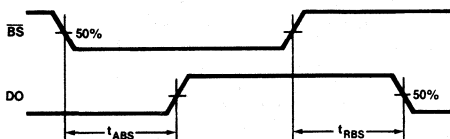
Write Mode



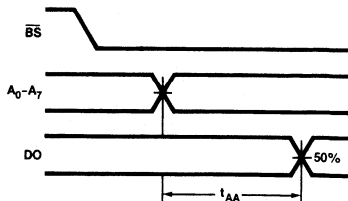
WF070105

NOTE:
All timing measurements referenced to 50% of input levels.

Input Levels



WF121905



WF122105

Read Mode

10422C 1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10422C device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratch pad, control, and buffer storage applications. The 10422C is available in a slimline 24-pin dual-in-line, flat or leadless package. This circuit may be reconfigured as 512×2 or 1024×1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The Open Emitter outputs have a 50Ω drive capability. The input pull-down resistor to V_{CC} is $50,000\Omega$ typical for the block selects.

Ordering information can be found on the following page.

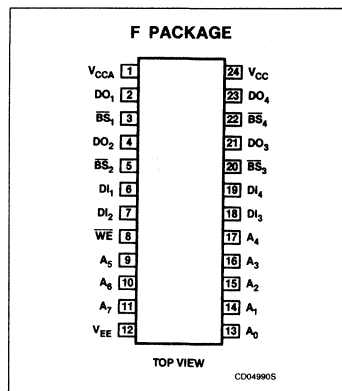
FEATURES

- 256 words \times 4 bits organization
- Fully compatible with 10K series ECL families
- Address access time:
- 10422C, 7ns max
- Low power dissipation of 0.8mW/bit
- Operating temperature: 0°C to $+75^\circ\text{C}$ (ambient)
- Block select allows variable organization

APPLICATIONS

- High speed scratch pad
- Control and buffer storage

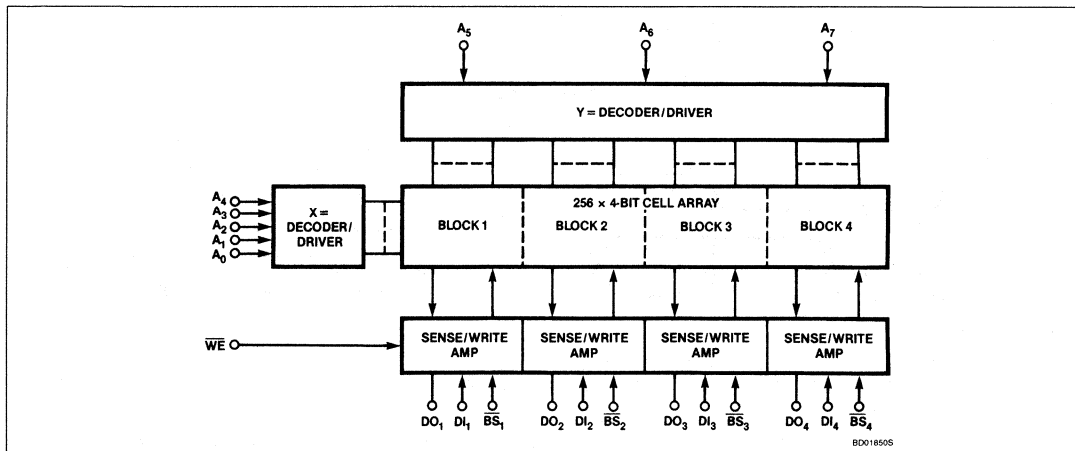
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{EE} Supply voltage	+0.5 to -7	V_{dc}
V_{IN} Input voltage	0 to V_{EE}	
I_O Output current	-30	mA
T_A Operating	0 to +75	$^\circ\text{C}$
T_J Operating junction	125	
T_{STG} Storage	-55 to +150	

BLOCK DIAGRAM



1K-Bit ECL Bipolar RAM (256 × 4)

10422C

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 400mil wide 24-pin	10422C F

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
		Min	Max	Min	Max	Min	Max	
Input voltage								
V_{IH} High		-1.145	-0.840	-1.105	-0.810	-1.045	-0.720	V
V_{IL} Low		-1.870	-1.490	-1.850	-1.475	-1.830	-1.450	
Output voltage								
V_{OH} High	$V_{IH} = \text{Max}$	-1.0	-0.840	-0.960	-0.810	-0.900	-0.720	V
V_{OL} Low	$V_{IL} = \text{Min}$	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	
V_{OHT} Threshold HIGH	$V_{IH} = \text{Min}$	-1.020		-0.980		-0.920		
V_{OLT} Threshold LOW	$V_{IL} = \text{Max}$		-1.645		-1.630		-1.605	
Input current								
I_{IH} High	$V_{IH} = \text{Max}$		220		220		220	μA
I_{IL} Low	$V_{IL} = \text{Min}$	-50		-50		-50		
I_{IL} BS	$V_{IL} = \text{Min}$	0.5		0.5		0.5		
I_{EE} Supply current	$V_{IL} = \text{Min}$		200		200		200	mA

NOTES:

1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_{AA}	Address access time			7	ns
T_{RBS}	Block select recovery time		4		
T_{ABS}	Block select access time		6		
T_{WD}	Write disable time		4		
T_{WPW}	Write pulse width	5			
T_{WR}	Write recovery time		6		
T_{WHA}	Address hold time		1		
T_{WHBS}	Block select hold time		1		
T_{WHD}	Data hold time		1		
T_{WSA}	Address set-up time		1		
T_{WSBS}	Block select set-up time		1		
T_{WSD}	Data set-up time		1		
t_f	Output fall time		2		
t_r	Output rise time		2		
Capacitance					pF
C_{IN}	Input			8	
C_{OUT}	Output			8	

NOTES:

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

1K-Bit ECL Bipolar RAM (256 × 4)

10422C

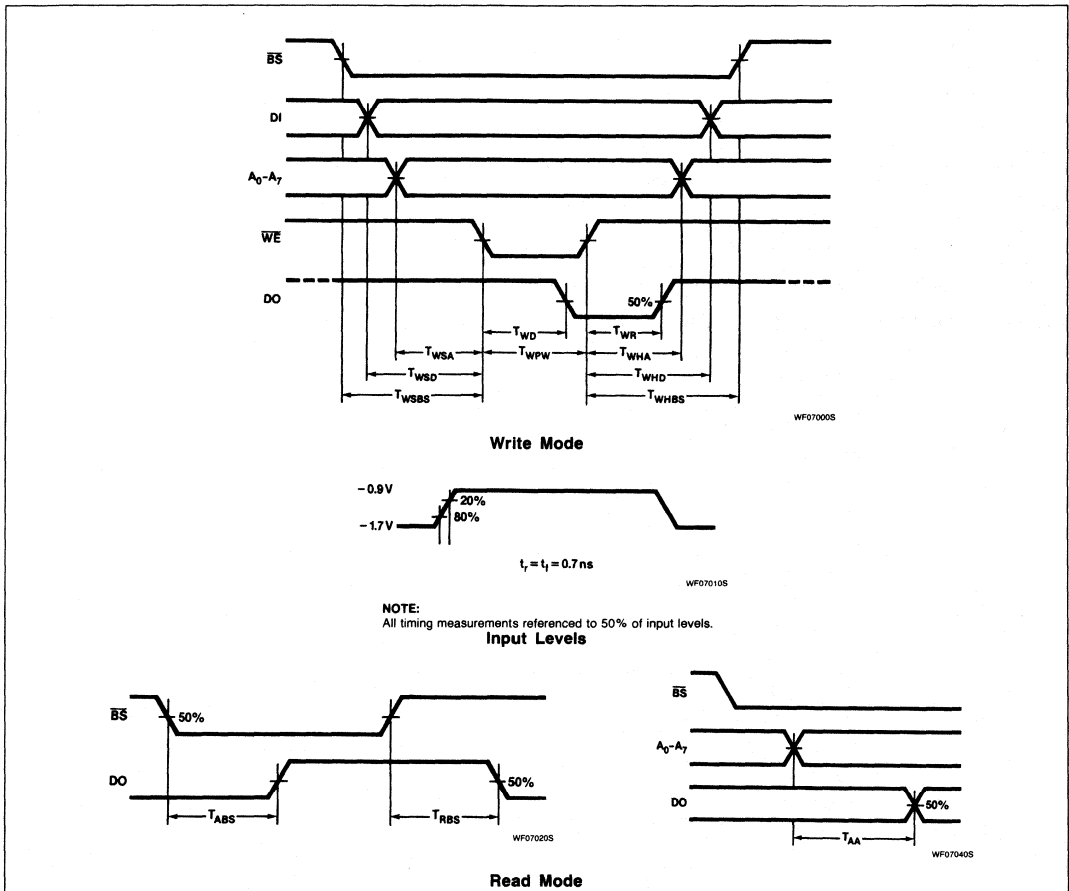
TRUTH TABLE

MODE	INPUTS			OUTPUTS
	\overline{BS}_N	WE	DI _N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D _{OUT}

NOTES:

- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- N = Blocks 1 - 4

TIMING DIAGRAMS



10470A 4K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10470A device is a 4096 words by 1 bit fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines, and an active LOW Chip Select input.

The 10470A is compatible with the 10K ECL families and includes on-chip voltage compensation for improved noise margin.

Ordering information can be found on the following page.

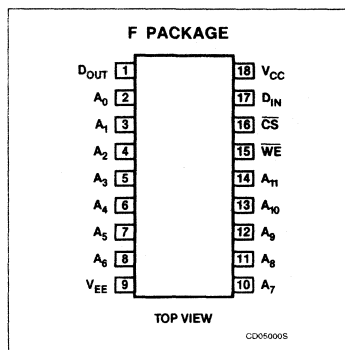
FEATURES

- Organization: 4096 words by 1 bit
- Fully compatible with 10K ECL families
- Operating temperature: 0°C to +75°C
- Address access time:
- 10470A: 15ns max
- Low supply current of 150mA max
- Read cycle time
- 10470A: 15ns

APPLICATIONS

- High speed scratch pad
- Control and buffer storage

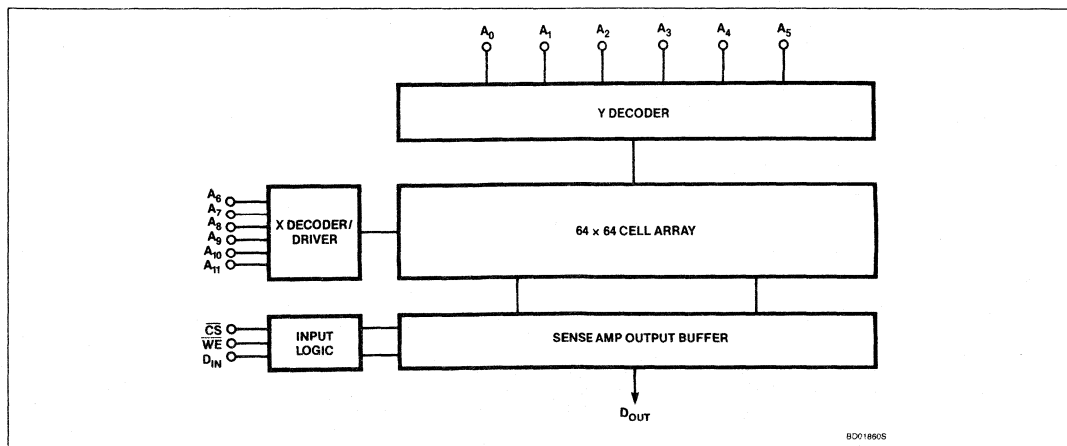
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	+0.5 to -7	V _{dc}
V _{IN} Input voltage	+0.5 to V _{EE}	
I _O Output current	-30	mA
T _A Operating	0 to +75	°C
T _{STG} Storage	-55 to +150	

BLOCK DIAGRAM



4K-Bit ECL Bipolar RAM (4096 × 1)

10470A

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 300mil wide 18-pin	10470A F

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
		Min	Max	Min	Max	Min	Max	
Input voltage V_{IH} High V_{IL} Low		-1.145 -1.870	-0.840 -1.490	-1.105 -1.850	-0.810 -1.475	-1.045 -1.830	-0.720 -1.450	V
Output voltage V_{OH} High V_{OL} Low V_{OHT} Threshold HIGH V_{OLT} Threshold LOW	$V_{IH} = \text{Max}$ $V_{IL} = \text{Min}$ $V_{IH} = \text{Min}$ $V_{IL} = \text{Max}$	-1.0 -1.870 -1.020	-0.840 -1.665 -1.645	-0.960 -1.850 -0.980	-0.810 -1.650 -1.630	-0.900 -1.830 -0.920	-0.720 -1.625 -1.605	V
Input current I_{IH} High I_{IL} Low I_{IL} CS	$V_{IH} = \text{Max}$ $V_{IL} = \text{Min}$ $V_{IL} = \text{Min}$	-50 0.5	220	-50 0.5	220	-50 0.5	220	μA
I_{EE} Supply current	$V_{IL} = \text{Min}$		150		150		150	mA

NOTES:

1. Voltages are defined with respect to ground, pin 18.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
T_{AA} Address access time			15	ns
T_{RCS} Chip select recovery time			5	
T_{ACS} Chip select access time			5	
T_{WD} Write disable time			6	
T_{WPW} Write pulse width	10			
T_{WR} Write recovery time			10	
T_{WHA} Address hold time	3			
T_{WHCS} Chip select hold time	3			
T_{WHD} Data hold time	3			
T_{WSA} Address set-up time	3			
T_{WSCS} Chip select set-up time	3			
T_{WSD} Data set-up time	3			
t_f Output fall time		1.5		
t_r Output rise time		1.5		
Capacitance				
C_{IN} Input			8	
C_{OUT} Output			8	

NOTES:

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

4K-Bit ECL Bipolar RAM (4096 × 1)

10470A

TRUTH TABLE

MODE	INPUTS			OUTPUTS
	\overline{CS}	\overline{WE}	D_{IN}	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

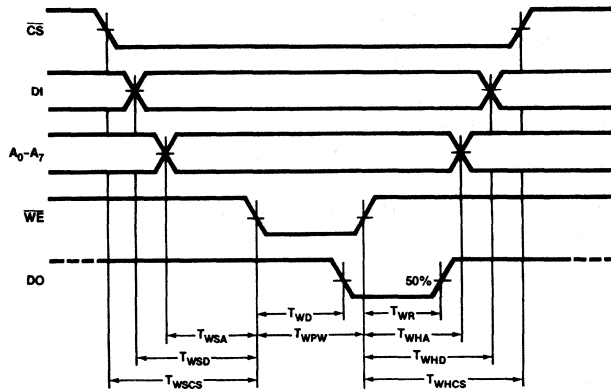
NOTES:

H = HIGH voltage level

L = LOW voltage level

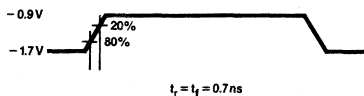
X = Don't care

TIMING DIAGRAMS



WF070505

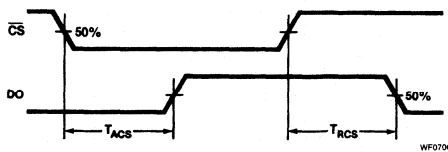
Write Mode



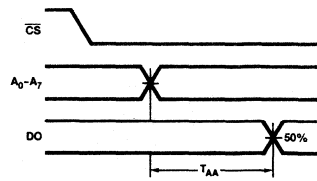
WF070105

NOTE: All timing measurements referenced to 50% of input levels.

Input Levels



WF070605



WF070705

Read Mode

100422B 1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100422B device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratchpad, control, and buffer storage applications. The 100422B contains voltage and temperature compensation circuits making it 100K family compatible. The 100422B is available in a slimline 24-pin dual-in-line package. This circuit may be reconfigured as 512×2 or 1024×1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable input and four Data outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply voltage. The input pull-down resistor to V_{EE} is $50,000\Omega$ typical for the block selects.

Ordering information can be found on the following page.

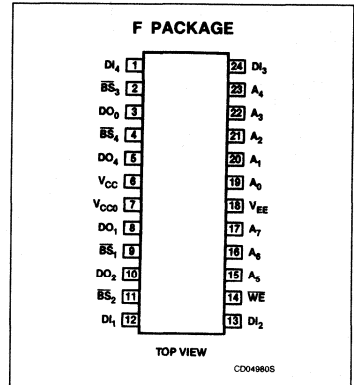
FEATURES

- 256 words \times 4 bits organization
- Fully compatible with 100K series ECL families
- Address access time:
- 100422B: 10ns max.
- Low power dissipation of 0.8mW/bit
- Operating temperature:
0°C to +85°C
- Block select allows variable organization

APPLICATIONS

- High-speed scratchpad
- Control and buffer storage

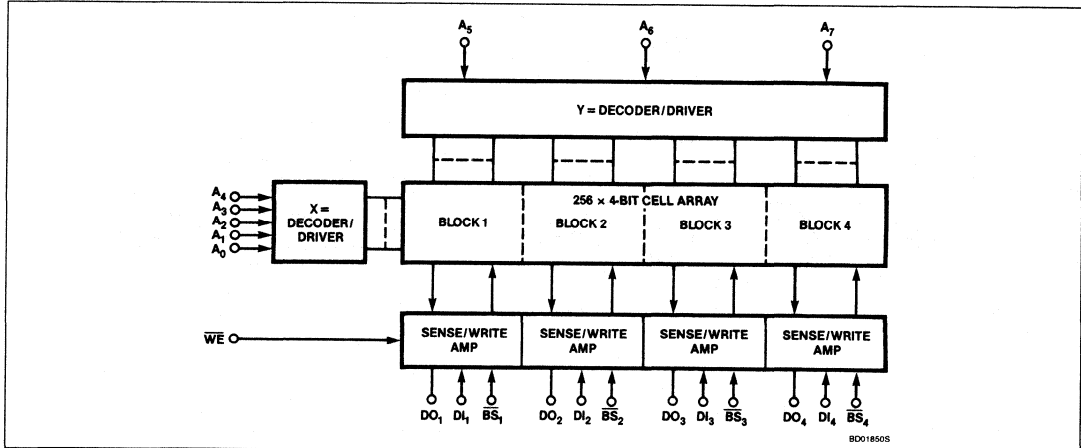
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{EE} Supply voltage	+0.5 to -7	V_{DC}
V_{IN} Input voltage	0 to V_{EE}	
I_O Output current	-30	mA
T_A Operating ambient temperature	0 to +85	°C
T_J Operating junction temperature	+125	
T_{STG} Storage temperature	-55 to +150	

BLOCK DIAGRAM



1K-Bit ECL Bipolar RAM (256 × 4)

100422B

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual-In-line 400mil wide 24-pin	100422B F

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V_{IL} Low V_{IH} High		-1.810 -1.165		-1.475 -0.880	V
Output voltage V_{OL} Low V_{OH} High V_{OLT} Threshold LOW V_{OHT} Threshold HIGH	$V_{IL} = \text{Min}$ $V_{IH} = \text{Max}$ $V_{IL} = \text{Max}$ $V_{IH} = \text{Min}$	-1.810 -1.025 -1.035	-1.715 -0.955	-1.620 -0.880 -1.610	V
Input current I_{iL} Low I_{iL} BS I_{iH} High	$V_{IL} = \text{Min}$ $V_{IL} = \text{Min}$ $V_{iH} = \text{Max}$	-50 +0.5		220	μA
I_{EE} Supply current				210	mA

NOTES:

1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{AA} Address access time				10	ns
t_{RBS} Block select recovery time				5	
t_{ABS} Block select access time				5	
t_{WD} Write disable time				5	
t_{WPW} Write pulse width	7				
t_{WR} Write recovery time			4.5	9	
t_{WHA} Address hold time	2	1			
t_{WHBS} Block select hold time	2	1			
t_{WHD} Data hold time	2	1			
t_{WSA} Address setup time	3	1			
t_{WSBS} Block select setup time	2	1			
t_{WSD} Data setup time	2	1			
t_f Output fall time		2			
t_r Output rise time		2			
Capacitance					pF
C_{iN} Input				8	
C_{oUT} Output				8	

NOTES:

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

1K-Bit ECL Bipolar RAM (256 × 4)

100422B

TRUTH TABLE

MODE	INPUTS			OUTPUTS
	\overline{BS}_N	WE	DI _N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D _{OUT}

NOTES:

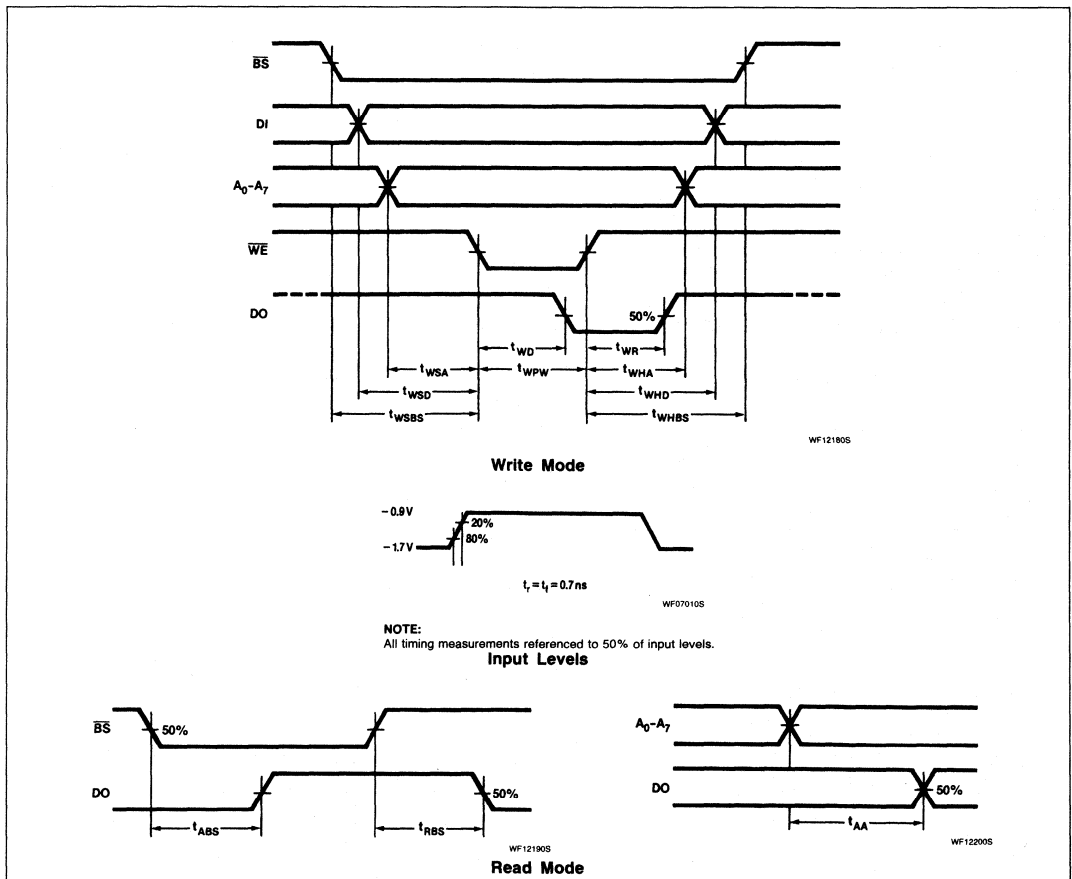
H = HIGH voltage level

L = LOW voltage level

X = Don't Care

N = Blocks 1-4

TIMING DIAGRAMS



100422C 1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100422C device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratch pad, control, and buffer storage applications. The 100422C contains voltage and temperature compensation circuits making it 100K family compatible. The 100422C is available in a slimline 24-pin dual-in-line package. This circuit may be reconfigured as 512×2 or 1024×1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply voltage. The input pull-down resistor to V_{EE} is $50,000\Omega$ typical for the block selects.

Ordering information can be found on the following page.

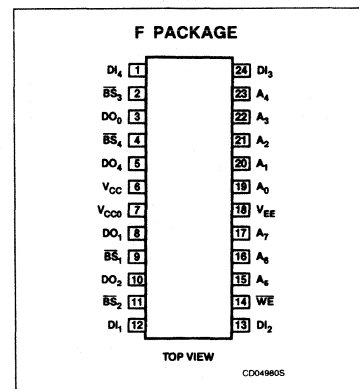
FEATURES

- 256 words \times 4 bits organization
- Fully compatible with 100K series ECL families
- Address access time:
- 100422C: 7ns max
- Low power dissipation of 0.8mW/bit
- Operating temperature: 0°C to $+85^\circ\text{C}$
- Block select allows variable organization

APPLICATIONS

- High speed scratch pad
- Control and buffer storage

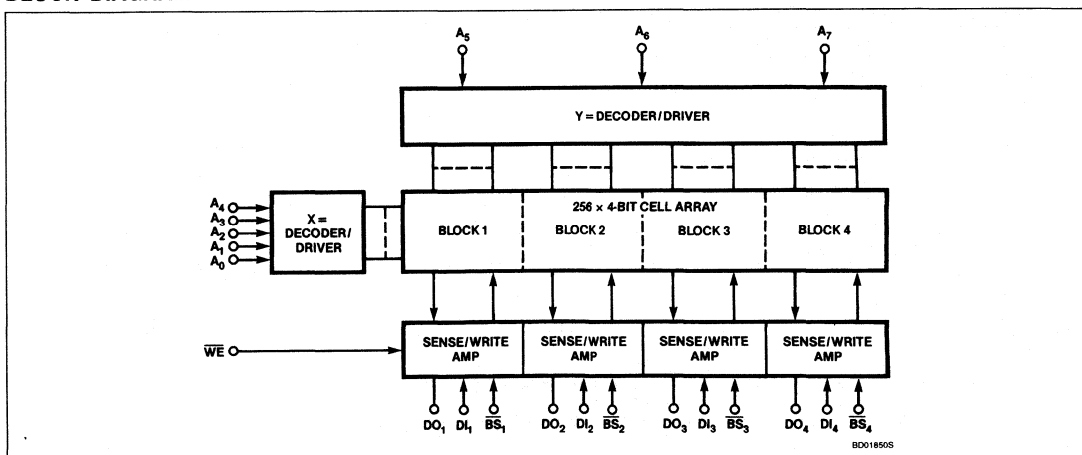
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{EE} Supply voltage	+0.5 to -7	V_{dc}
V_{IN} Input voltage	0 to V_{EE}	
I_O Output current	-30	mA
T_A Operating	0 to +85	$^\circ\text{C}$
T_J Operating junction	+125	
T_{STG} Storage	-55 to +150	

BLOCK DIAGRAM



1K-Bit ECL Bipolar RAM (256 × 4)

100422C

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 400mil wide 24-pin	100422C F

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V_{IL} Low V_{IH} High		-1.810 -1.165		-1.475 -0.880	V
Output voltage V_{OL} Low V_{OH} High V_{OLT} Threshold LOW V_{OHT} Threshold HIGH	$V_{IL} = \text{Min}$ $V_{IH} = \text{Max}$ $V_{IL} = \text{Max}$ $V_{IH} = \text{Min}$	-1.810 -1.025 -1.035	-1.715 -0.955	-1.620 -0.880 -1.610	V
Input current I_{IL} Low I_{IL} BS I_{IH} High	$V_{IL} = \text{Min}$ $V_{IL} = \text{Min}$ $V_{IH} = \text{Max}$	-50 +0.5		220	μA
I_{EE} Supply current				210	mA

NOTES:

1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
T_{AA} Address access time			7	ns
T_{RBS} Block select recovery time		4		
T_{ABS} Block select access time		6		
T_{WD} Write disable time		4		
T_{WPW} Write pulse width	5			
T_{WR} Write recovery time		6		
T_{WHA} Address hold time		1		
T_{WHBS} Block select hold time		1		
T_{WHD} Data hold time		1		
T_{WSA} Address set-up time		1		
T_{WSBS} Block select set-up time		1		
T_{WSD} Data set-up time		1		
t_f Output fall time		2		
t_r Output rise time		2		
Capacitance C_{IN} Input C_{OUT} Output			8 8	pF

NOTES:

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

1K-Bit ECL Bipolar RAM (256 × 4)

100422C

TRUTH TABLE

MODE	INPUTS			OUTPUTS
	\overline{BS}_N	WE	DI_N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:

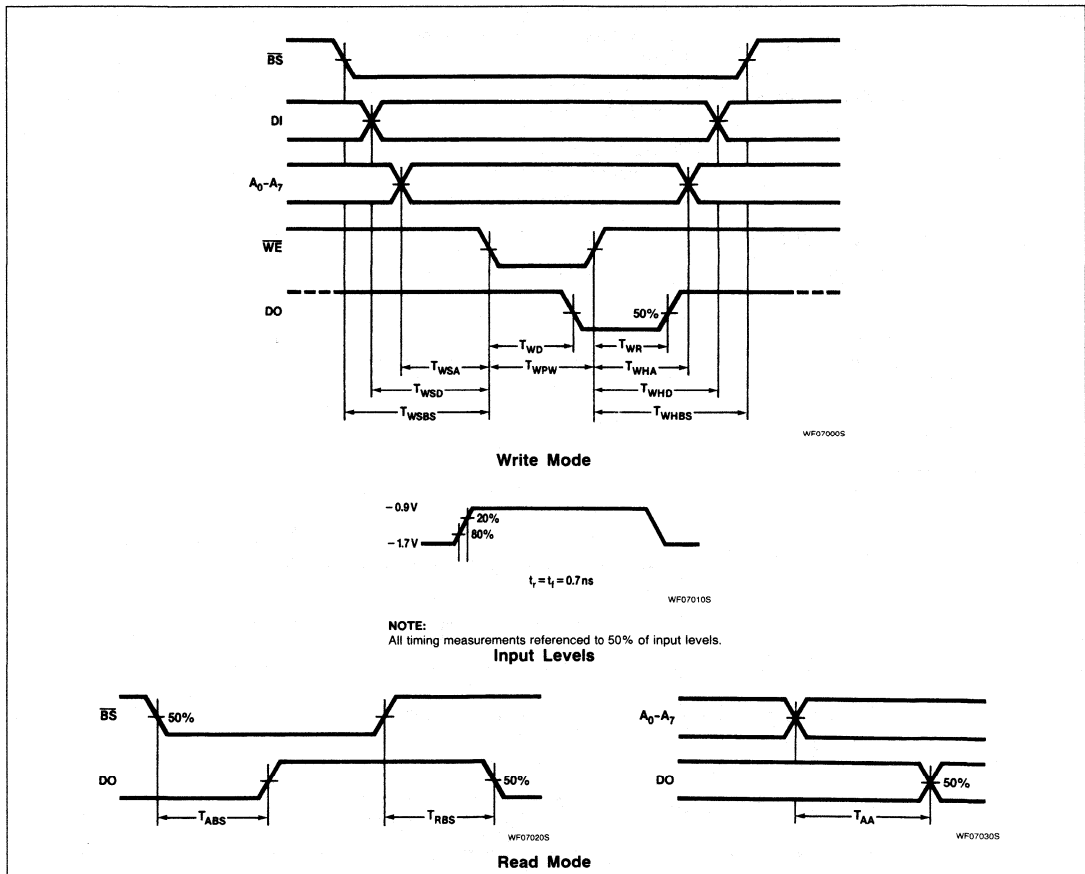
H = HIGH voltage level

L = LOW voltage level

X = Don't care

N = Blocks 1 - 4

TIMING DIAGRAMS



100470A 4K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100470A device is a 4096 words by 1 bit fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines, and an active LOW Chip Select Input.

The 100470A is compatible with the 100K ECL families and includes on-chip voltage and temperature compensation.

Ordering information can be found on the following page.

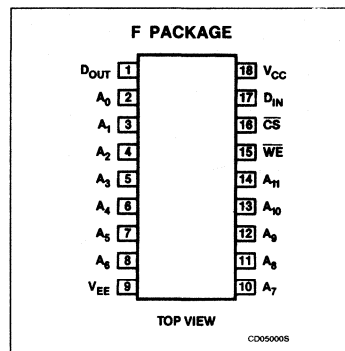
FEATURES

- Organization: 4096 words by 1 bit
- Fully compatible with 100K ECL families
- Operating temperature: 0°C to +85°C
- Address access time:
- 100470A: 15ns max
- Low supply current of 150mA max
- Read cycle time:
- 100470A: 15ns max

APPLICATIONS

- High speed scratch pad
- Control and buffer storage

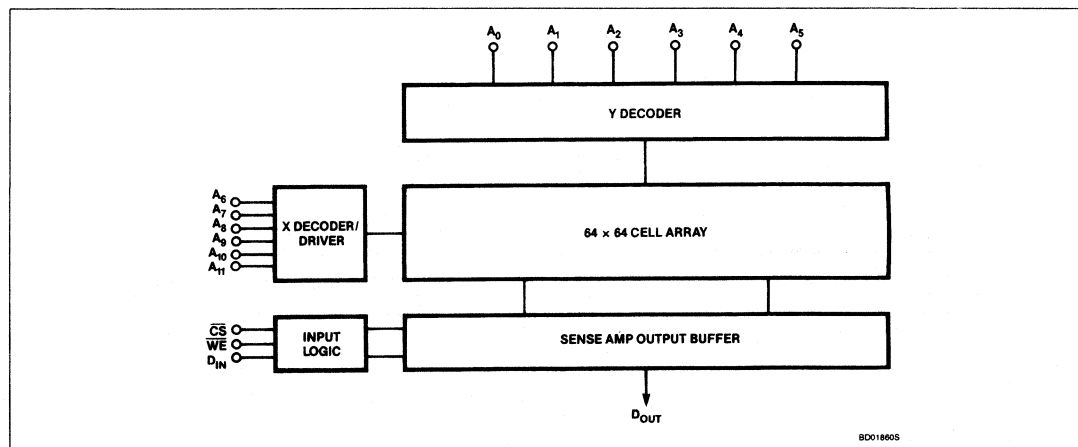
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	+0.5 to -7	V _{dc}
V _{IN} Input voltage	+0.5 to V _{EE}	
I _O Output current	-30	mA
T _A Operating	0 to +85	°C
T _{STG} Storage	-55 to +150	

BLOCK DIAGRAM



4K-Bit ECL Bipolar RAM (4096 × 1)

100470A

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 300mil wide 18-pin	100470A F

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V_{IL} Low V_{IH} High		-1.810 -1.165		-1.475 -0.880	V
Output voltage V_{OL} Low V_{OH} High V_{OLT} Threshold LOW V_{OHT} Threshold HIGH	$V_{IL} = \text{Min}$ $V_{IH} = \text{Max}$ $V_{IL} = \text{Max}$ $V_{IH} = \text{Min}$	-1.810 -1.025 -1.035	-1.715 -0.955	-1.620 -0.880 -1.610	V
Input current I_{IL} Low I_{IL} CS I_{IH} High	$V_{IL} = \text{Min}$ $V_{IL} = \text{Min}$ $V_{IH} = \text{Max}$	-50 +0.5		220	μA
I_{EE} Supply current				150	mA

NOTES:

1. Voltages are defined with respect to ground, pin 18.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
T_{AA} Address access time			15	ns
T_{RCS} Chip select recovery time			5	
T_{ACS} Chip select access time			5	
T_{WD} Write disable time			6	
T_{WPW} Write pulse width	10			
T_{WR} Write recovery time			10	
T_{WHA} Address hold time	3			
T_{WHCS} Chip select hold time	3			
T_{WHD} Data hold time	3			
T_{WSA} Address set-up time	3			
T_{WSCS} Chip select set-up time	3			
T_{WSD} Data set-up time	3			
t_f Output fall time		1.5		
t_r Output rise time		1.5		
Capacitance C_{IN} Input C_{OUT} Output			8 8	pF

NOTES:

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

4K-Bit ECL Bipolar RAM (4096 × 1)

100470A

TRUTH TABLE

MODE	INPUTS			OUTPUTS
	\overline{CS}	\overline{WE}	D_{IN}	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

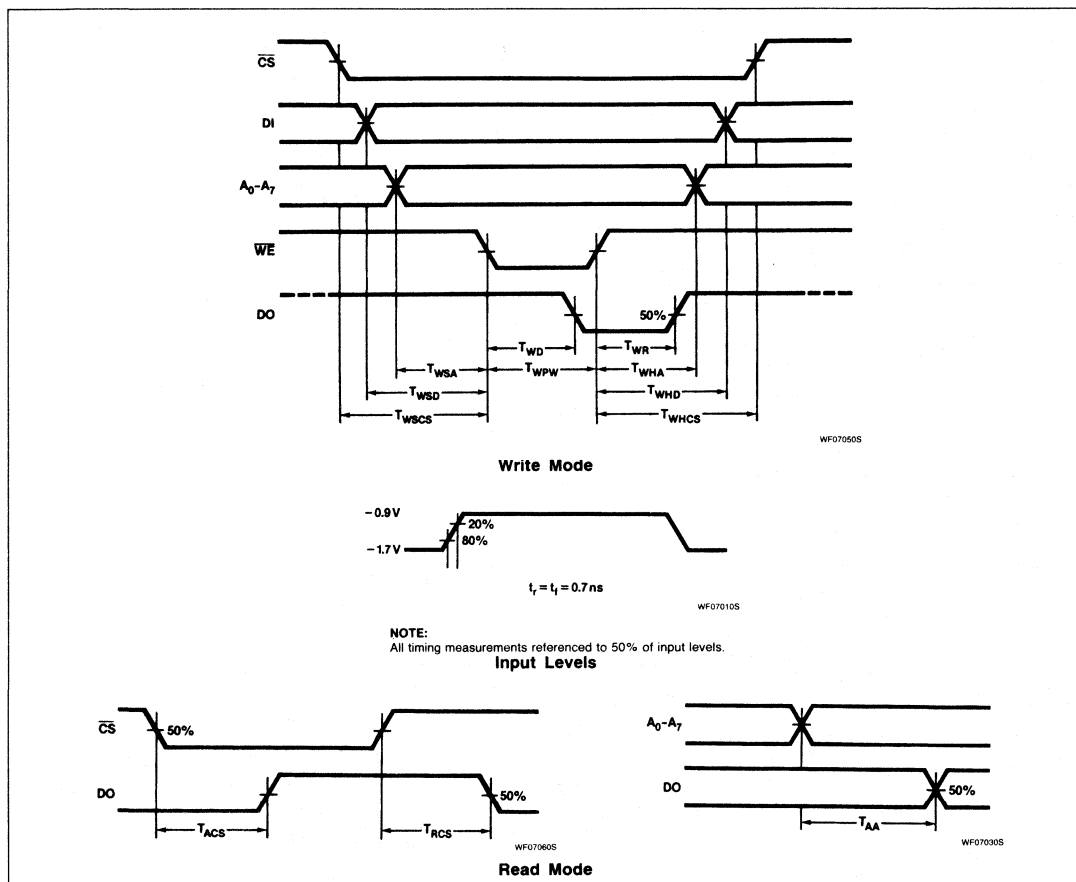
NOTES:

H = HIGH voltage level

L = LOW voltage level

X = Don't care

TIMING DIAGRAMS



100474A

4K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100474A device is a 1024 words by 4 bits fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines.

The 100474A, with its voltage and temperature compensation, is compatible with the 100K ECL families.

Ordering information can be found on the following page.

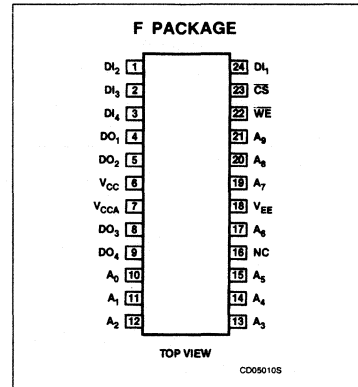
FEATURES

- Organization: 1024 words by 4 bits
- Fully compatible with 100K ECL families
- Operating temperature: 0°C to +85°C
- Address access time:
- 100474A: 15ns max
- Low supply current of 210mA max
- Read Cycle time:
- 100474A: 15ns

APPLICATIONS

- High speed scratch pad
- Control and buffer storage

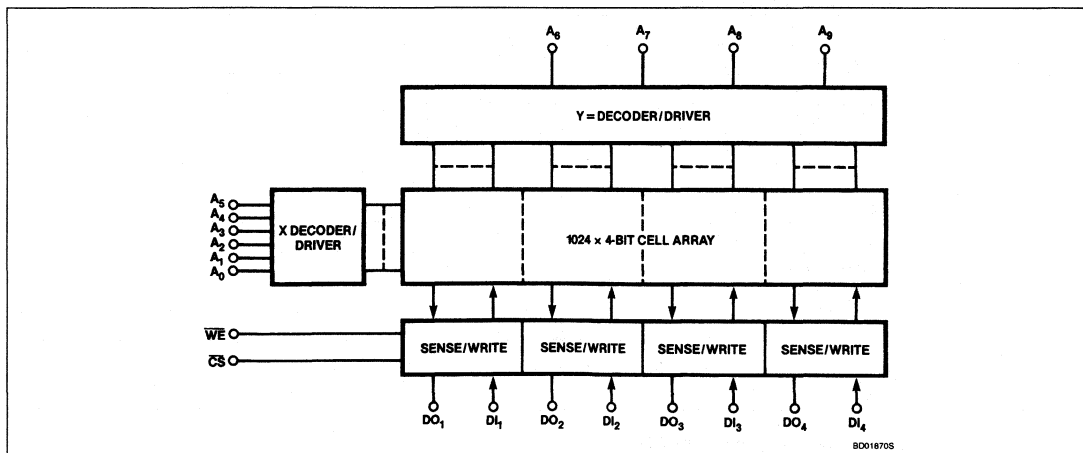
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	+0.5 to -7	V _{dc}
V _{IN} Input voltage	+0.5 to V _{EE}	
I _O Output current	-30	mA
T _A Operating	0 to +85	°C
T _{stg} Storage	-55 to +150	

BLOCK DIAGRAM



4K-Bit ECL Bipolar RAM (1024 × 4)

100474A

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 400mil wide 24-pin	100474A F

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V_{IL} Low V_{IH} High		-1.810 -1.165		-1.475 -0.880	V
Output voltage V_{OL} Low V_{OH} High V_{OLT} Threshold LOW V_{OHT} Threshold HIGH	$V_{IL} = \text{Min}$ $V_{IH} = \text{Max}$ $V_{IL} = \text{Max}$ $V_{IH} = \text{Min}$	-1.810 -1.025 -1.035	-1.715 -0.955	-1.620 -0.880 -1.610	V
Input current I_{IL} Low I_{IL} BS I_{IH} High	$V_{IL} = \text{Min}$ $V_{IL} = \text{Min}$ $V_{IH} = \text{Max}$	-50 +0.5		220	μA
I_{EE} Supply current				210	mA

NOTES:

1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, T_A = 0^\circ C$ to $85^\circ C$

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_{AA}	Address access time			15	ns
T_{RCS}	Chip select recovery time			5	
T_{ACS}	Chip select access time			5	
T_{WD}	Write disable time			6	
T_{WPW}	Write pulse width	10			
T_{WR}	Write recovery time			10	
T_{WHA}	Address hold time	3			
T_{WHCS}	Chip select hold time	3			
T_{WHD}	Data hold time	3			
T_{WSA}	Address set-up time	3			
T_{WSCS}	Chip select set-up time	3			
T_{WSD}	Data set-up time	3			
t_f	Output fall time		1.5		
t_r	Output rise time		1.5		
Capacitance					μF
C_{IN}	Input			8	
C_{OUT}	Output			8	

NOTES:

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

4K-Bit ECL Bipolar RAM (1024 × 4)

100474A

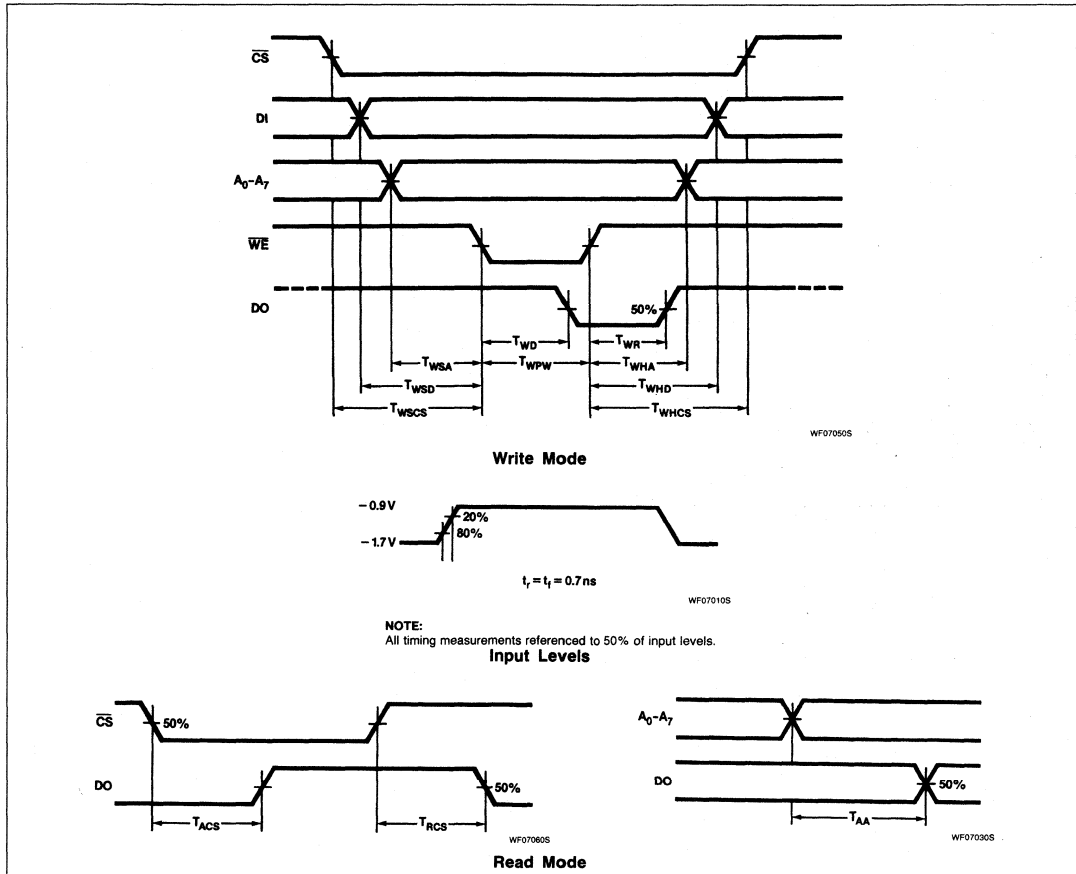
TRUTH TABLE

MODE	INPUTS			OUTPUTS
	\overline{CS}	\overline{WE}	D_{IN}	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

TIMING DIAGRAMS



PACKAGE INFORMATION

Package outlines	325
Introduction	326
Package outlines for product with prefixes: HEF, PCA, PCB, PCD, PCF, SAA, SBB	341
Introduction	341

Package Outlines

Introduction	326
Leaded Chip Carrier	327
SO-L Dual in-Line	328
Cerdip	330
Dual in-Line	335

Bipolar Memory Products

INTRODUCTION

The following information applies to packages currently used for Bipolar Memories. For information on other package configurations, refer to the respective Data Manual for each product.

GENERAL

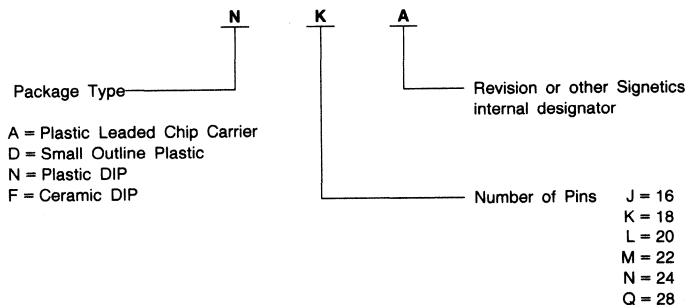
1. The following pages contain information on plastic DIP and cerdip packages ranging from 16 pins to 28 pins. In addition, the SO-L 16- and 20-pin and the 28-pin Leaded Chip Carrier,

have been added since the last printing of this manual.

- Information for each set of drawings such as notes and reference standards precede each section for easy reference.
- Thermal resistance values have been determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC}

and ground. Since thermal resistance values are dependent on die size and the value of power dissipated, measurements were made on packages containing various die sizes. The information in the tables shown here are typical values for a mid bipolar memory die size for a given package. For more detailed information on thermal performance of specific packages please contact your Signetics sales representative and request the latest publication of Thermal performance data.

Assembly Package codes consist of two or three alphas as follows:



Note that ordering codes use only the package type alpha as shown above with the addition of a number to clarify the width of the 24-pin DIPs, i.e., N3 or F3 when both widths are available in a single device type.

Package Outlines

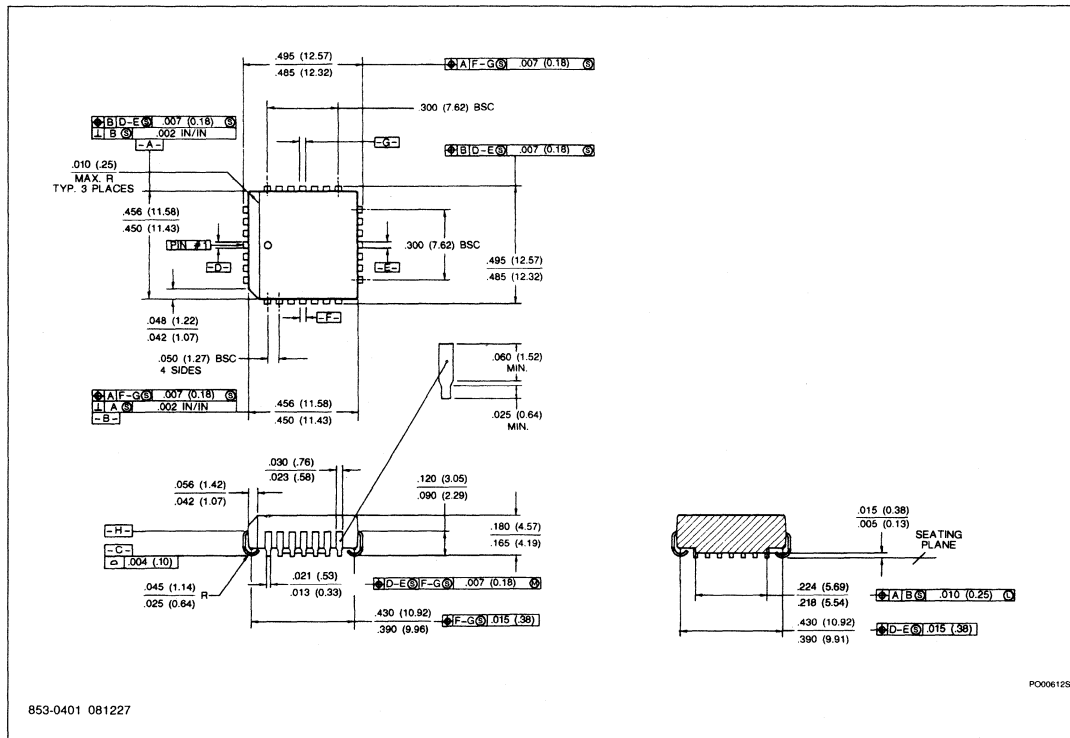
PLASTIC PLCC

1. Package dimensions conform to JEDEC specifications for standard Leaded Chip Carrier outline (PLCC) package.
2. Controlling dimensions are given in inches with dimensions in millimeters contained in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
4. "D-E" and "F-G" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
6. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
7. Body material: Plastic (Epoxy).
8. Thermal test Fixture: Device soldered to a glass epoxy test board with the following dimensions 1.58" x 0.75" x 0.059" with 0.009" stand off.

PLASTIC LEADED CHIP CARRIER

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
28	AQ	60/24	0.450 in. sq.

AQ1 PLASTIC PLCC-28



Package Outlines

PLASTIC SO-LS

1. Package dimensions conform to JEDEC specifications for standard small outline (SO-L) packages (issue A June 1985).
2. Controlling dimensions are given in millimeters, mm, with dimensions in inches contained in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
6. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
7. Body material: Plastic (Epoxy).
8. Thermal test fixture: Device soldered to a glass epoxy test board with the dimensions of 1.58" × 0.75" × 0.059" with 0.009" stand off.

PLASTIC SMALL OUTLINE PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	DJ	95/30	300 mil wide
20	DL	86/24	300 mil wide

Package Outlines

HERMETIC CERDIP

- Package dimensions conform to JEDEC specifications for standard Ceramic Dual Inline (Cerdip) package.
- Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
- Dimensioning and tolerancing per ANSI Y14.5M - 1982.
- Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
- These dimensions measured with the leads constrained to be perpendicular to plane T.
- Lead material: ASTM alloy F-30 (Alloy 42) or equivalent - tin plated or solder dipped.
- Body Material: Ceramic with glass seal at leads.
- Thermal test fixture: Device secured in Textool ZIF socket with 0.04" stand off.

CERAMIC DUAL-IN-LINE PACKAGES

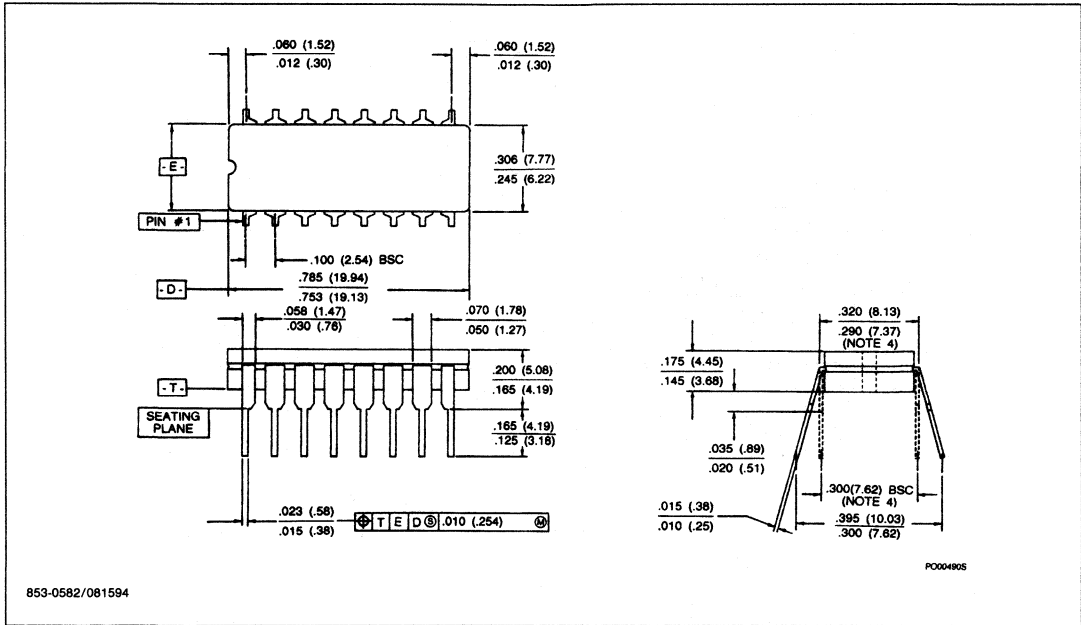
NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	FJD	77/30	300 mil wide
18	FKD	73/27	300 mil wide
20	FLD	72/25	300 mil wide
22	FM	66/27	400 mil wide
24	FNM ¹	63/26	300 mil wide
24	FND	62/26	600 mil wide
28	FQD	57/27	600 mil wide

NOTES:

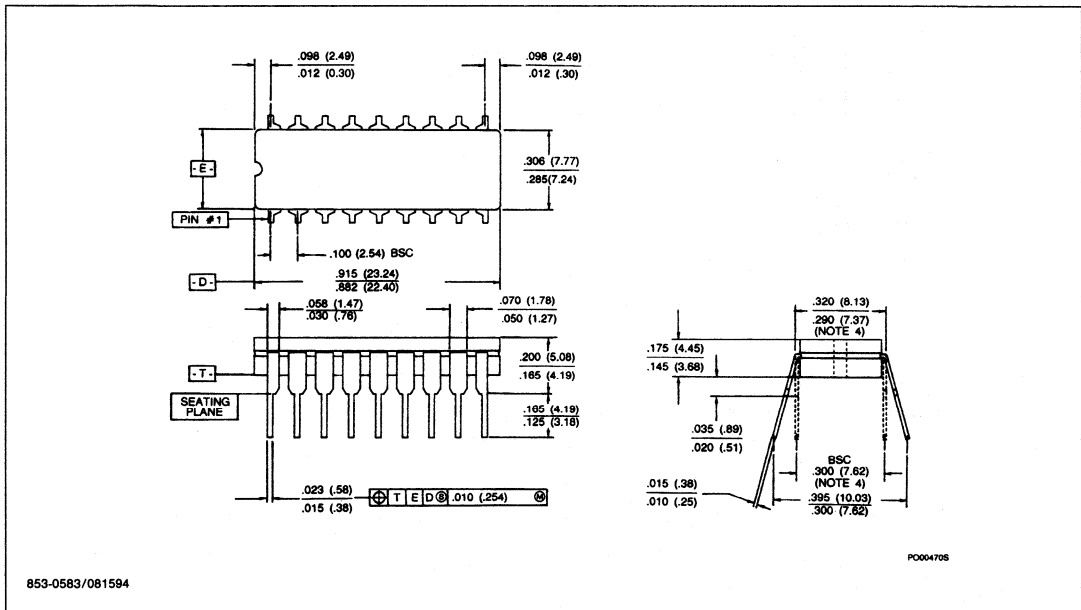
- Order coded as N3

Package Outlines

FJ1 HERMETIC CDIP-16

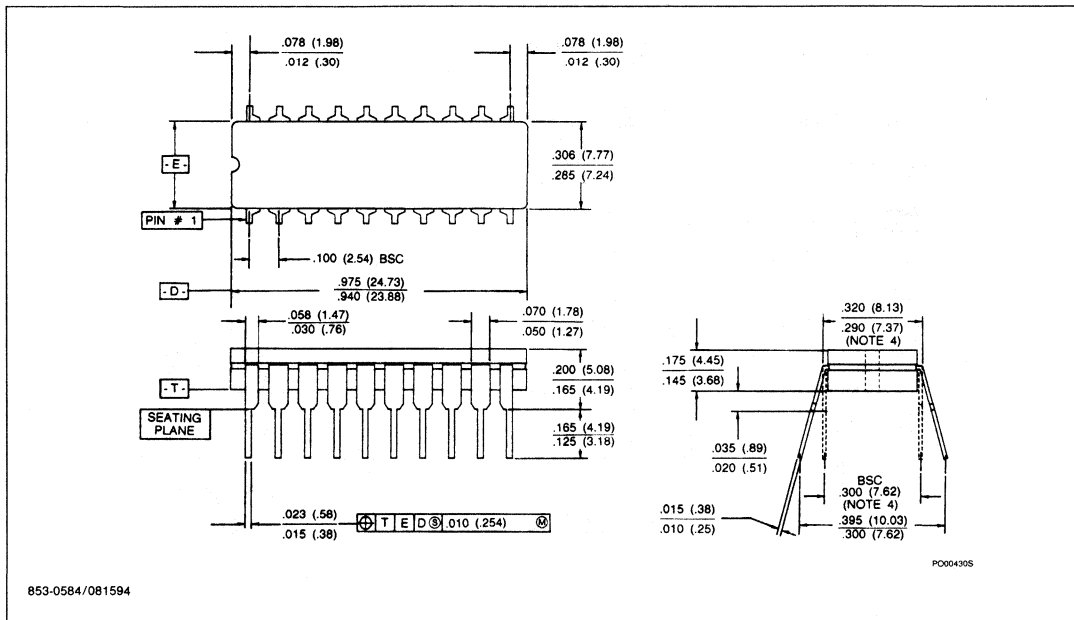


FK1 HERMETIC CDIP-18

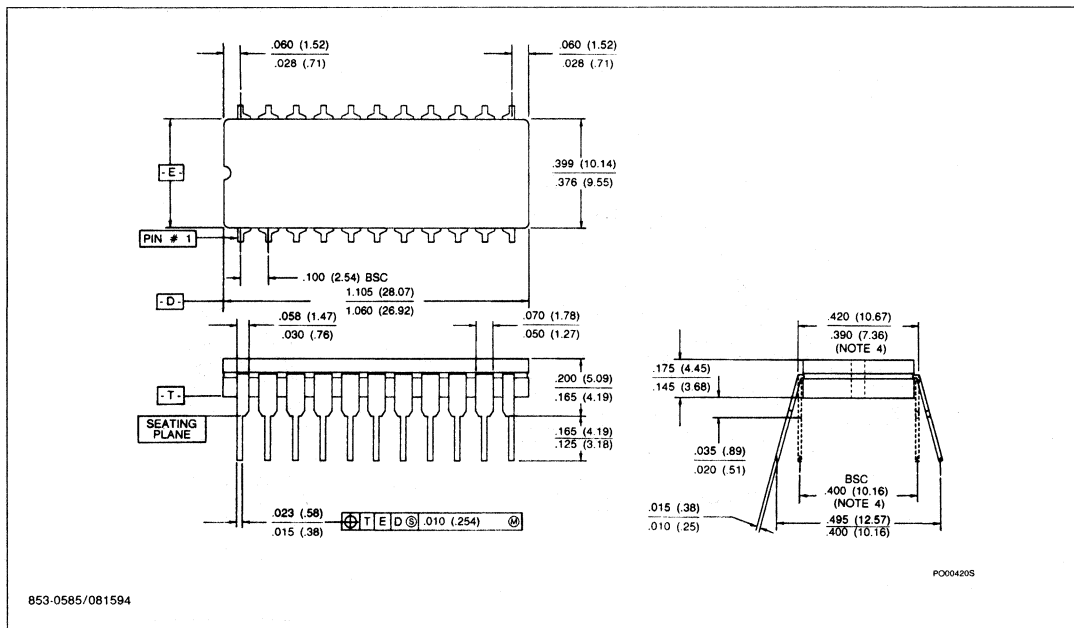


Package Outlines

FL1 HERMETIC CDIP-20

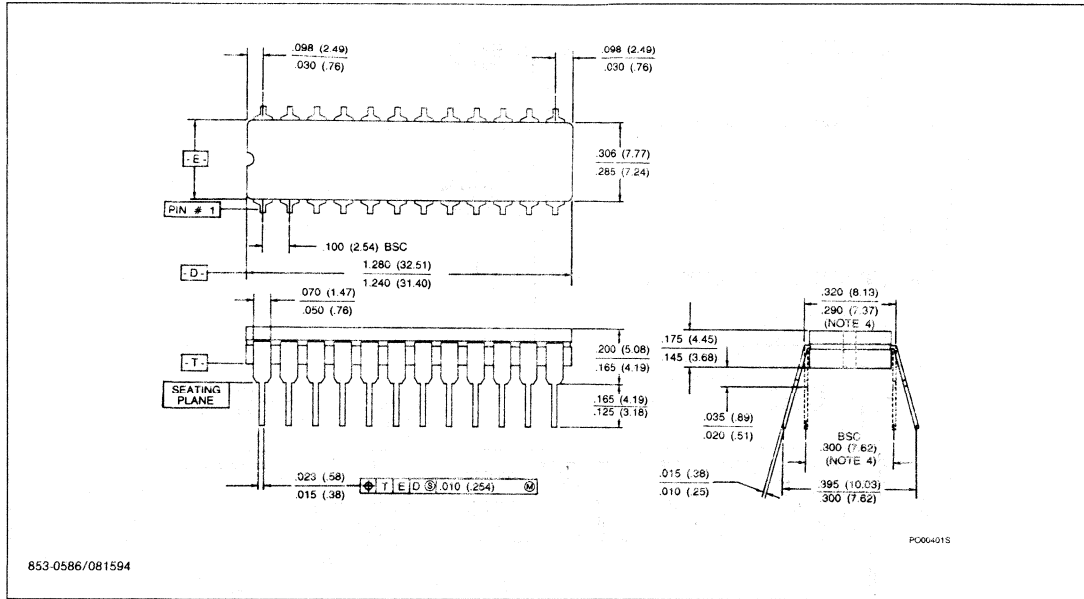


FM2 HERMETIC CDIP-22

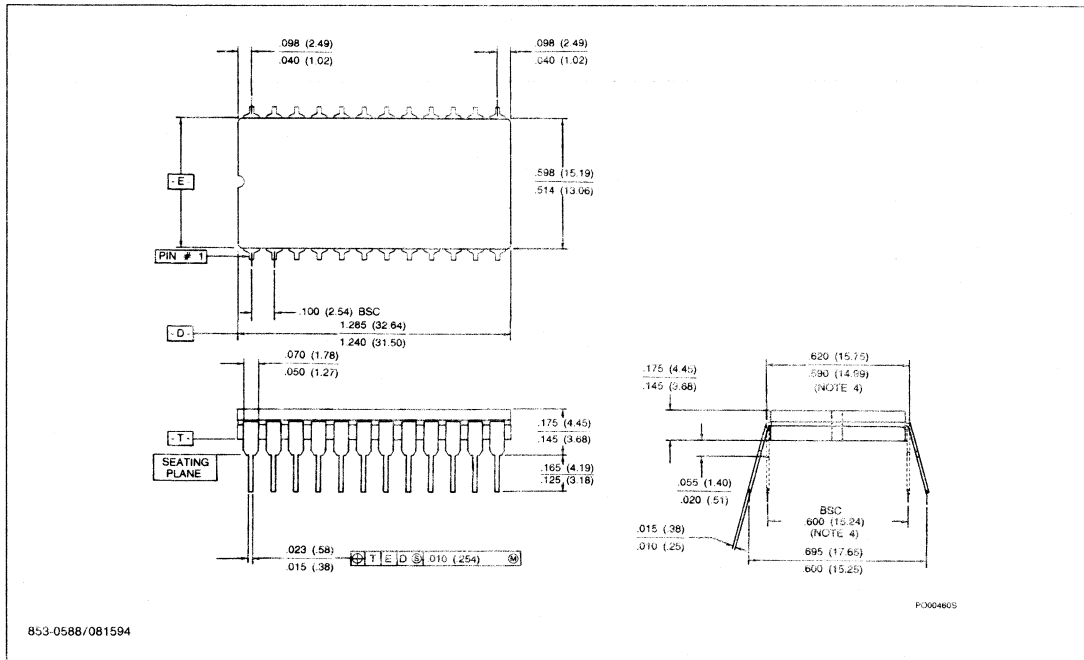


Package Outlines

FN1 HERMETIC CDIP-24



FN3 HERMETIC CDIP-24



Package Outlines

PLASTIC DIP

- Package dimensions conform to JEDEC specification MS-001-AA for standard Plastic Dual Inline (DIP) package.
- Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
- Dimensioning and tolerancing per ANSI Y14.5M - 1982.
- "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.01 inch (0.25mm) on any side.
- These dimensions measured with the leads constrained to be perpendicular to plane T.
- Pin numbers start with pin # 1 and continue counterclockwise when viewed from the top.
- Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
- Body material: Plastic (Epoxy)
- Thermal test fixture: Device secured in a Textool ZIF socket with 0.04" stand off.

PLASTIC DUAL-IN-LINE PACKAGES

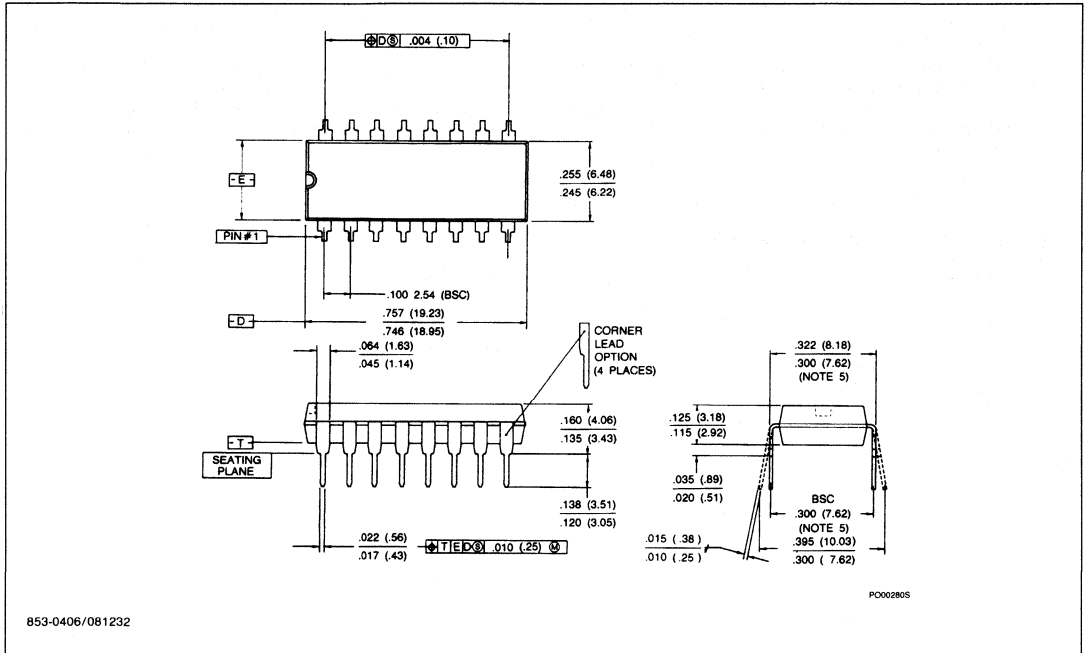
NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	NJD	76/26	300 mil wide
18	NKD	63/24	300 mil wide
20	NLD	60/24	300 mil wide
22	NM	54/20	400 mil wide
24	NNM ¹	46/18	300 mil wide
24	NND	44/18	600 mil wide
28	NQD	42/16	600 mil wide

NOTES:

- Order coded as N3

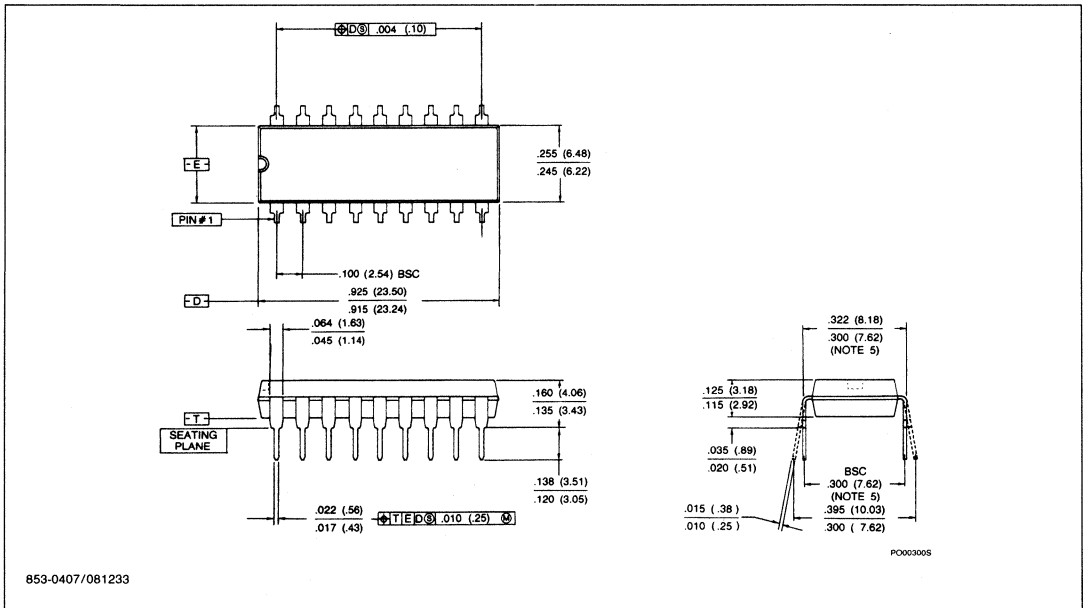
Package Outlines

NJ1 PLASTIC PDIP-16



853-0406/081232

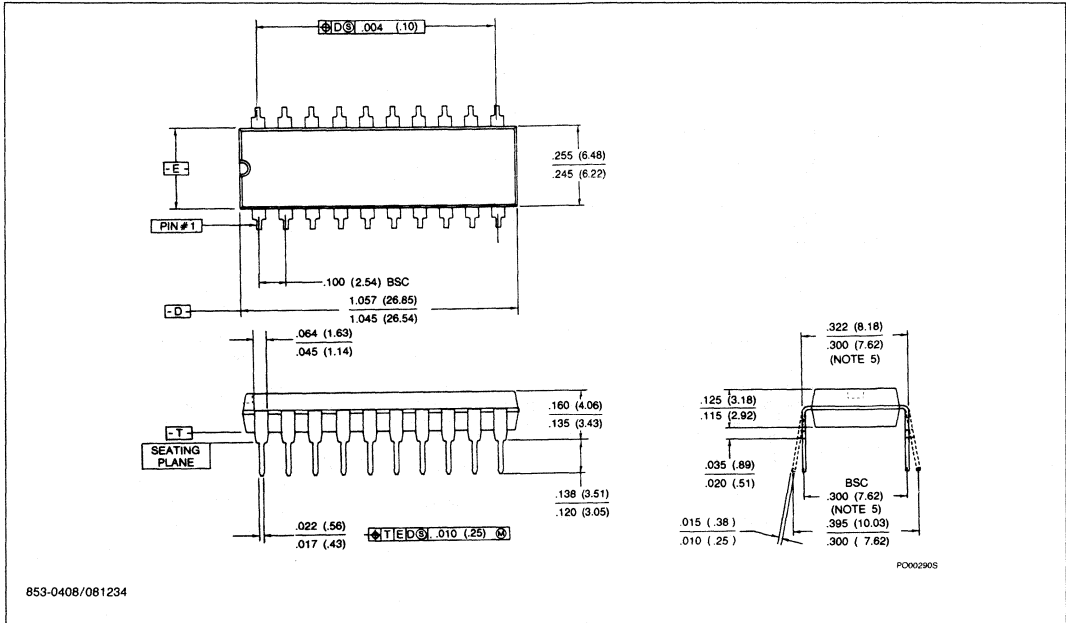
NK1 PLASTIC PDIP-18



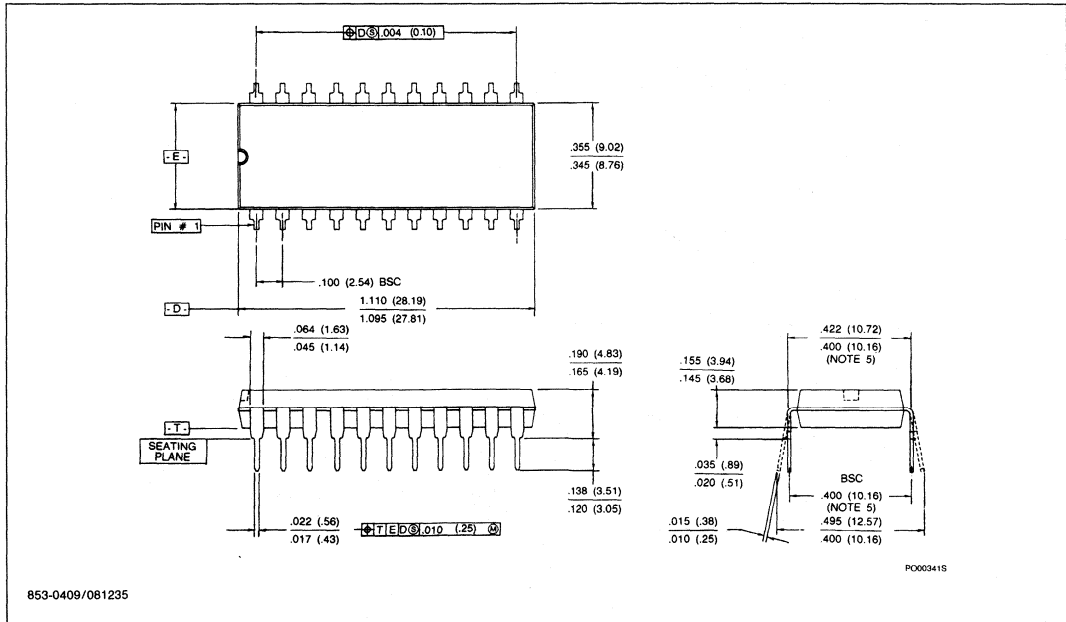
853-0407/081233

Package Outlines

NL1 PLASTIC PDIP-20

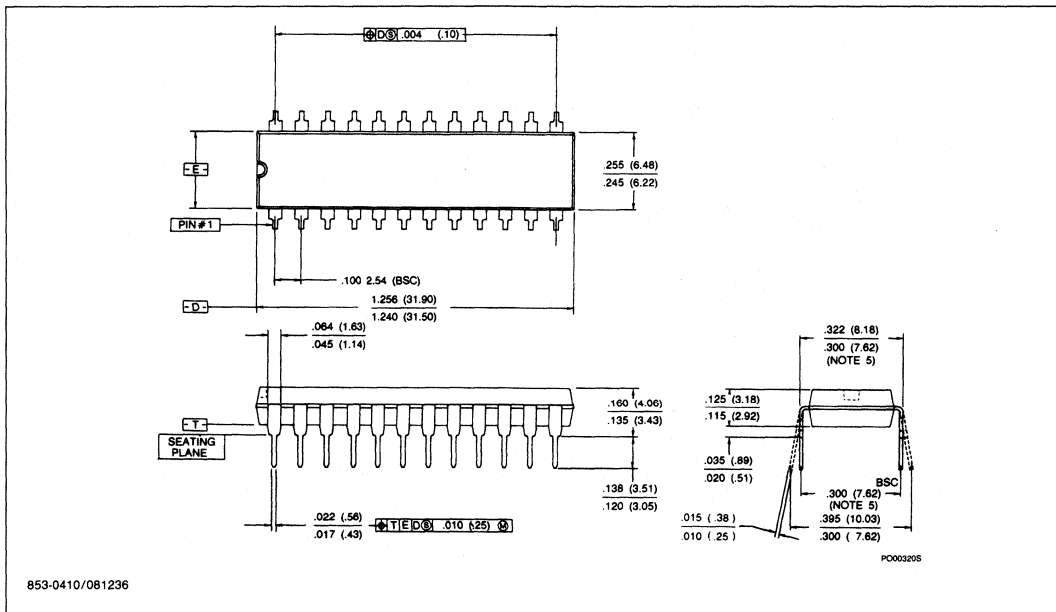


NM2 PLASTIC PDIP-22

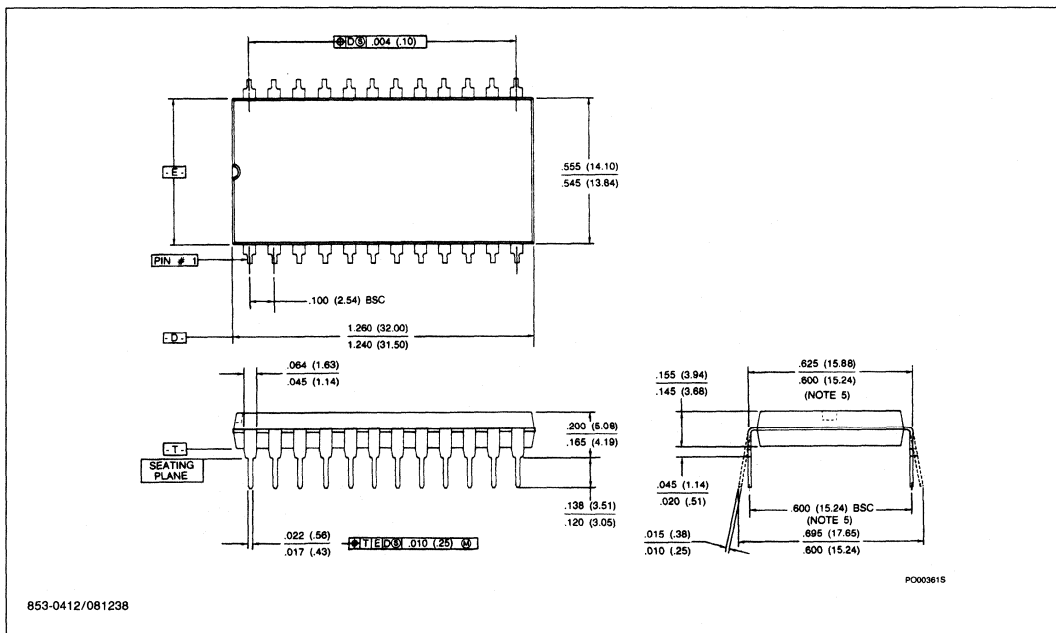


Package Outlines

NN1 PLASTIC PDIP-24

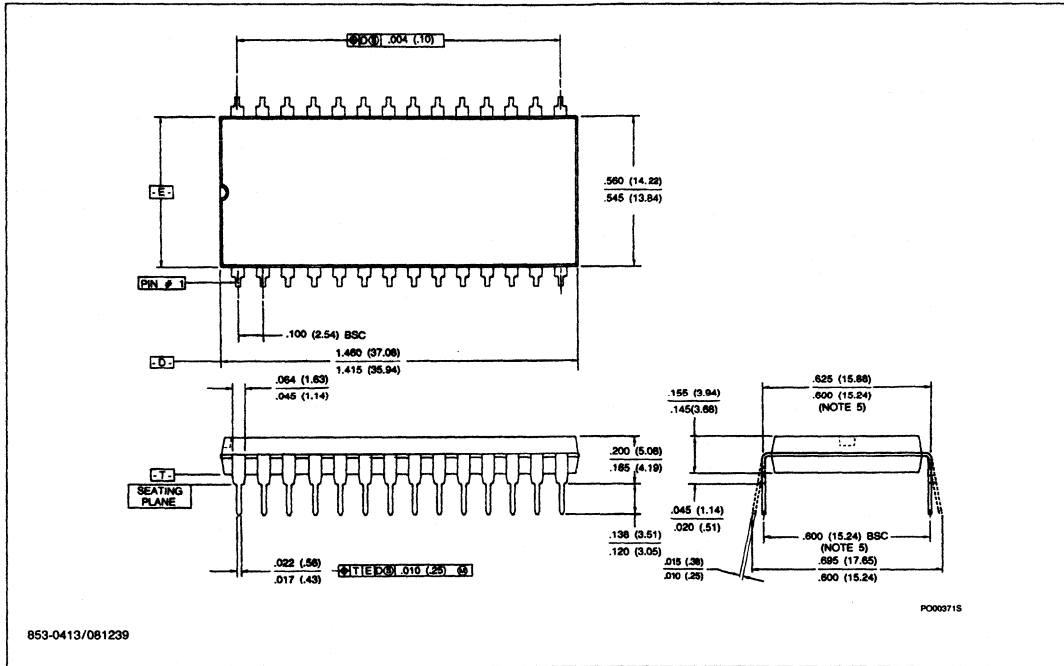


NN3 PLASTIC PDIP-24



Package Outlines

NQ3 PLASTIC PDIP-28



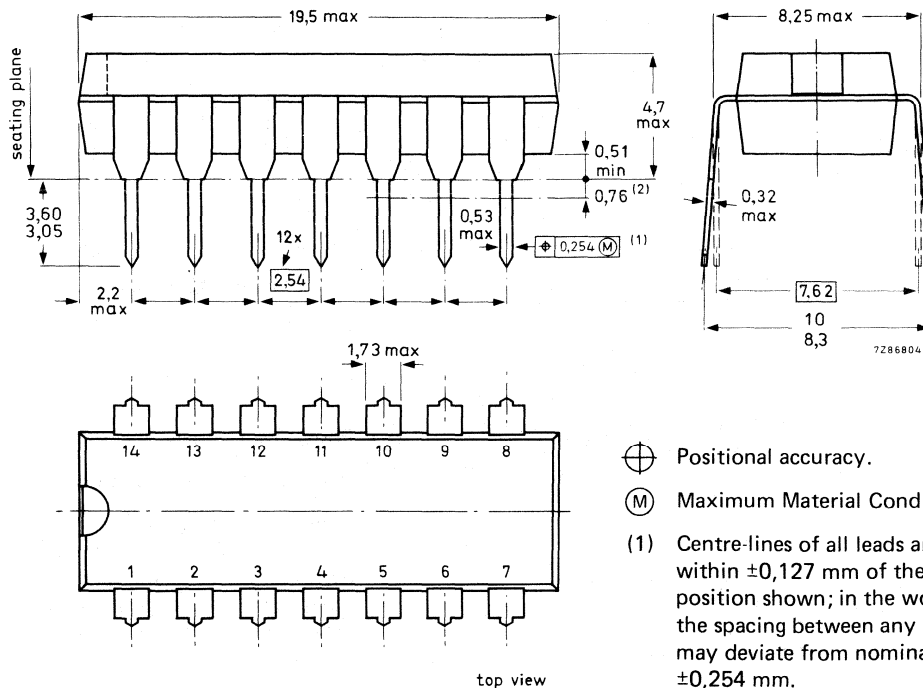
PACKAGE OUTLINES

Introduction
for Prefixes: HEF, PCA, PCB, PCD, PCF, SAA, SBB.341

The package information for each type number is given below:

type number	description and package code	page
HEF4505BP	14-lead dual in-line; plastic (SOT-27KE, ME, MF)	343
HEF4505BD	14-lead dual in-line; ceramic (cerdip) (SOT-73A, B, C)	345
HEF4720BP	16-lead dual in-line; plastic (SOT-38ZE)	344
HEF4720VP	16-lead dual in-line; plastic (SOT-38ZE)	344
HEF4720BD	16-lead dual in-line; ceramic (cerdip) (SOT-74A, B, C)	347
HEF4720VD	16-lead dual in-line; ceramic (cerdip) (SOT-74A, B, C)	347
HEF4720BT	16-lead mini-pack; plastic (SO-16L; SOT-162A)	355
HEF4720VT	16-lead mini-pack; plastic (SO-16L; SOT-162A)	355
PCB8582P	8-lead dual in-line; plastic (SOT-97AE,DE,EE)	348
PCD5101P	22-lead dual in-line; plastic (SOT-116)	351
PCD5101T	24-lead mini-pack; plastic (SO-24; SOT-137A)	354
PCD5114D	18-lead dual in-line; ceramic (cerdip) (SOT-133B)	353
PCD5114P	18-lead dual in-line; plastic (SOT-102NE,GE,PE)	350
PCD5114T	20-lead mini-pack; plastic (SO-20; SOT-163A)	356
PCF8570P	8-lead dual in-line; plastic (SOT-97AE,DE,EE)	348
PCF8570T	8-lead mini-pack; plastic (SO-8L; SOT-176)	357
PCF8571P	8-lead dual in-line; plastic (SOT-97AE,DE,EE)	348
PCF8571T	8-lead mini-pack; plastic (SO-8L; SOT-176)	357
PCF8583P	8-lead dual in-line; plastic (SOT-97AE,DE,EE)	348
PCF8583T	8-lead mini-pack; plastic (SO-8L; SOT-176)	357
SAA9001PB	28-lead dual in-line; plastic (SOT-117)	352
SAA9001EB	28-lead dual in-line; metal ceramic (cerdip) (SOT-87B)	346
SBB6116LP	24-lead dual in-line; plastic (SOT-101A, B, C, F, G, L)	349

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27KE, ME, MF)



- ⊕ Positional accuracy.
 - Ⓜ Maximum Material Condition.
- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
 - (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

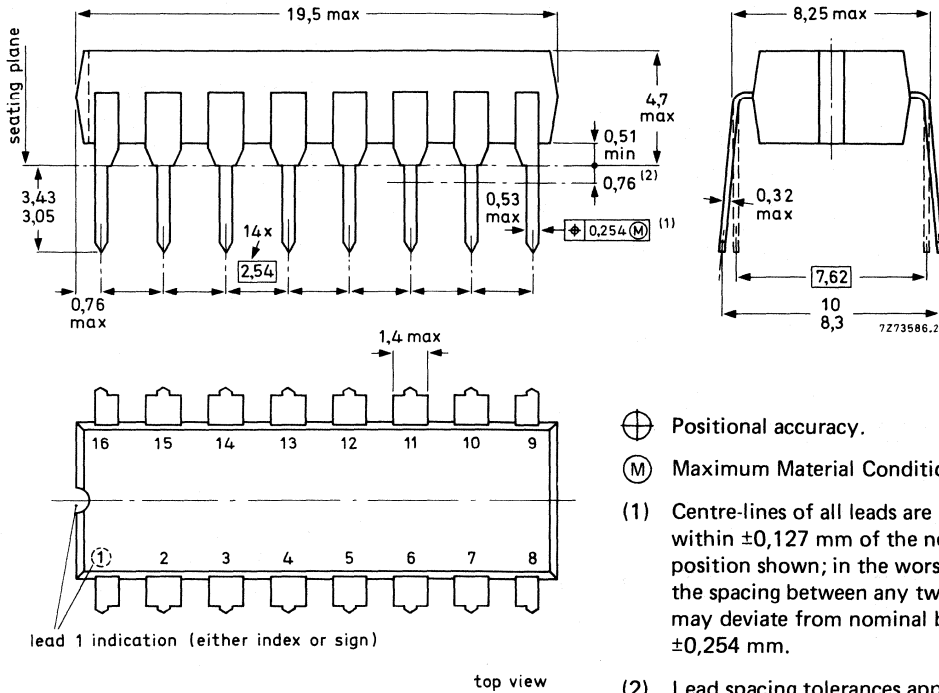
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38ZE)



lead 1 indication (either index or sign)

top view

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.
- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

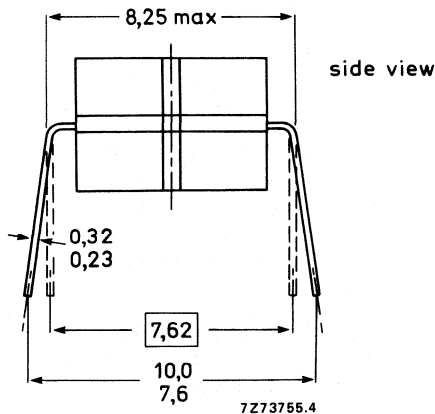
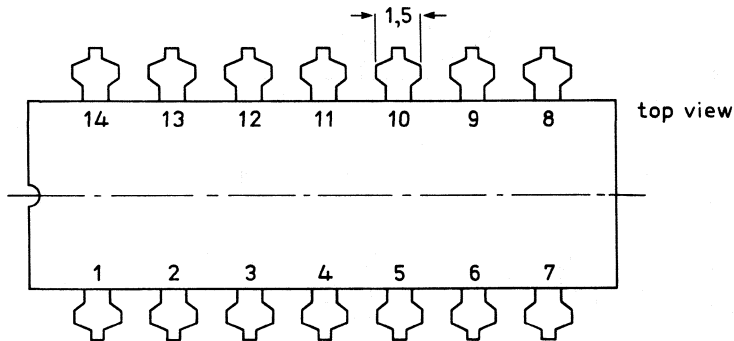
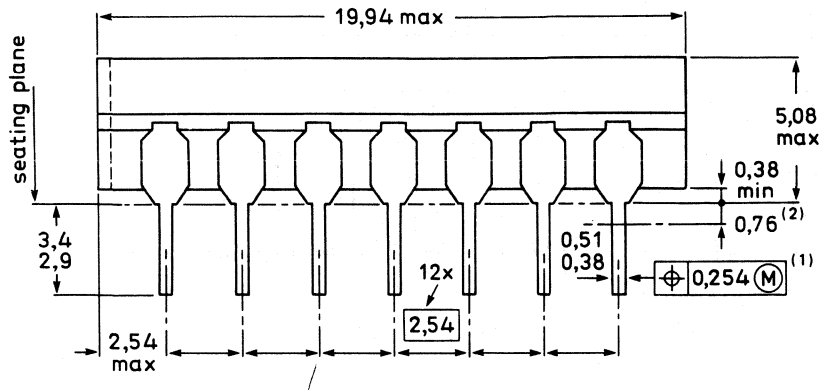
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

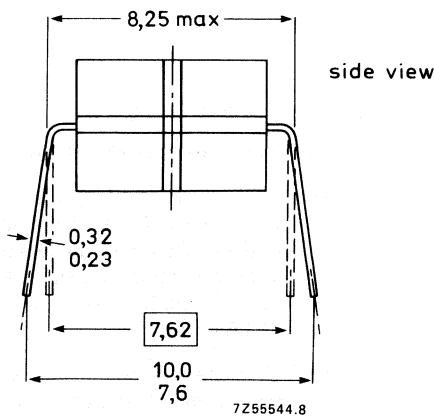
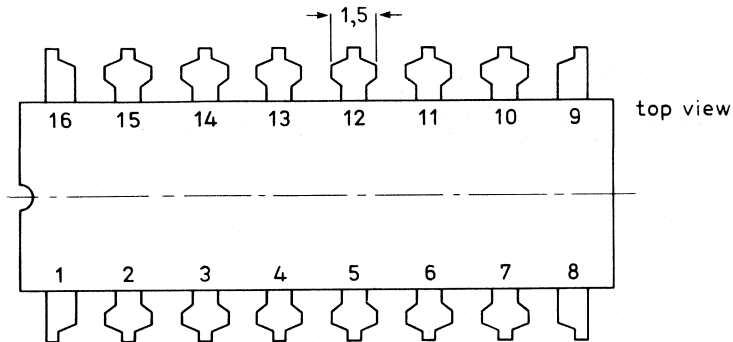
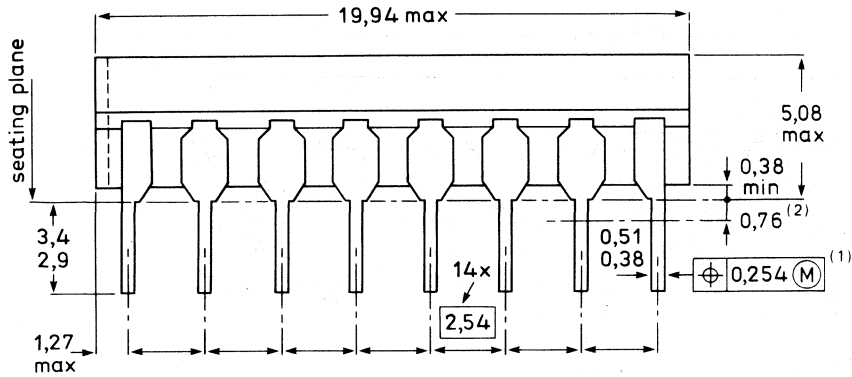
14-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-73A,B,C)



- ⊕ Positional accuracy.
 (M) Maximum Material Condition.
- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-74A,B,C)

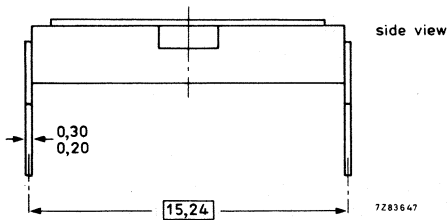
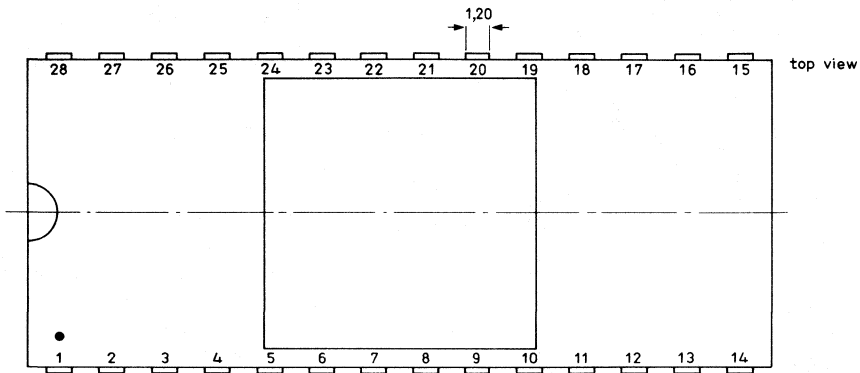
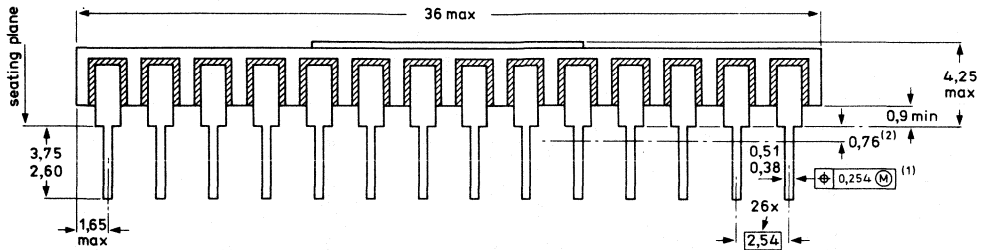


- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-87B)



Dimensions in mm

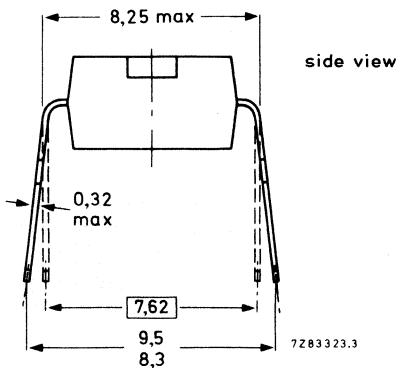
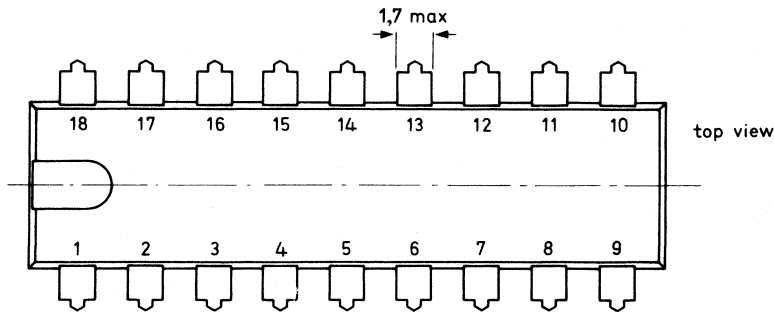
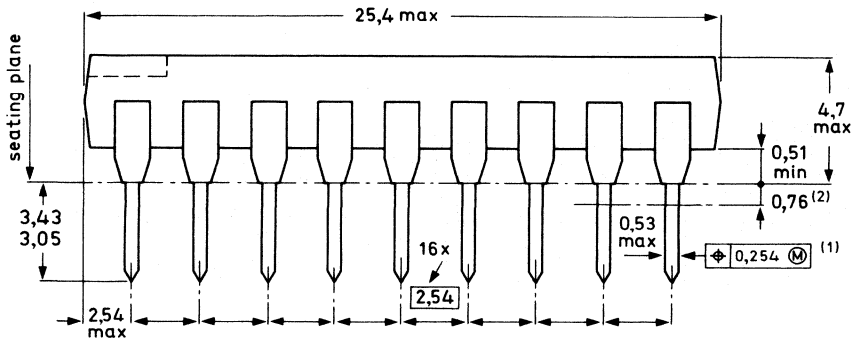
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102AE, GE, PE)



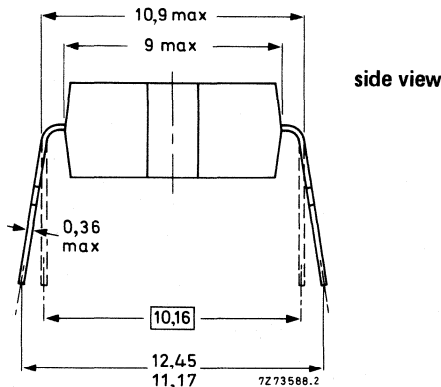
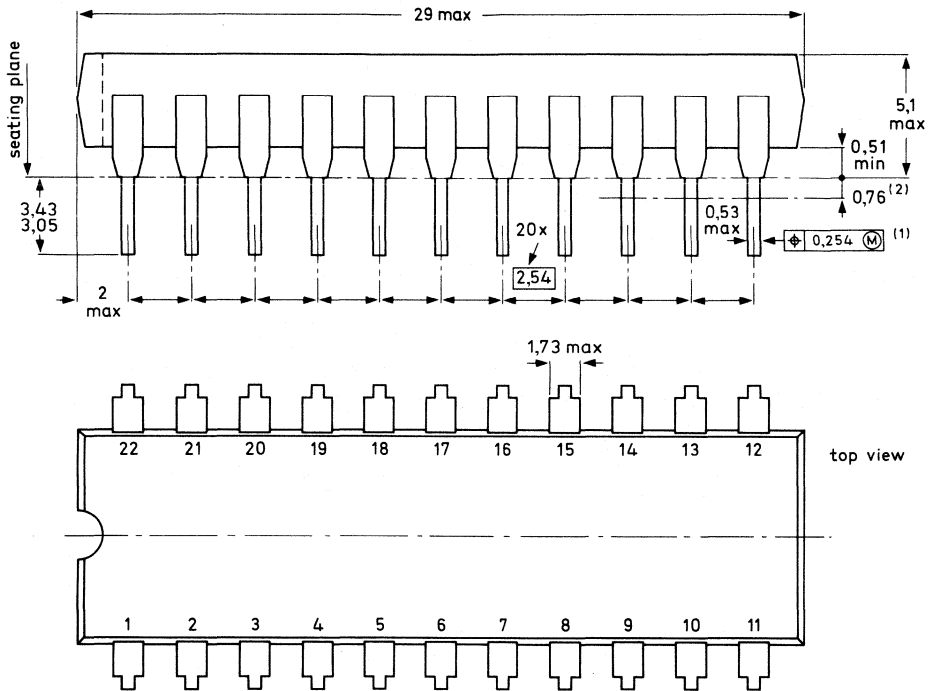
- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING
See page 358

22-LEAD DUAL IN-LINE; PLASTIC (SOT-116)



\oplus Positional accuracy.

\textcircled{M} Maximum Material Condition.

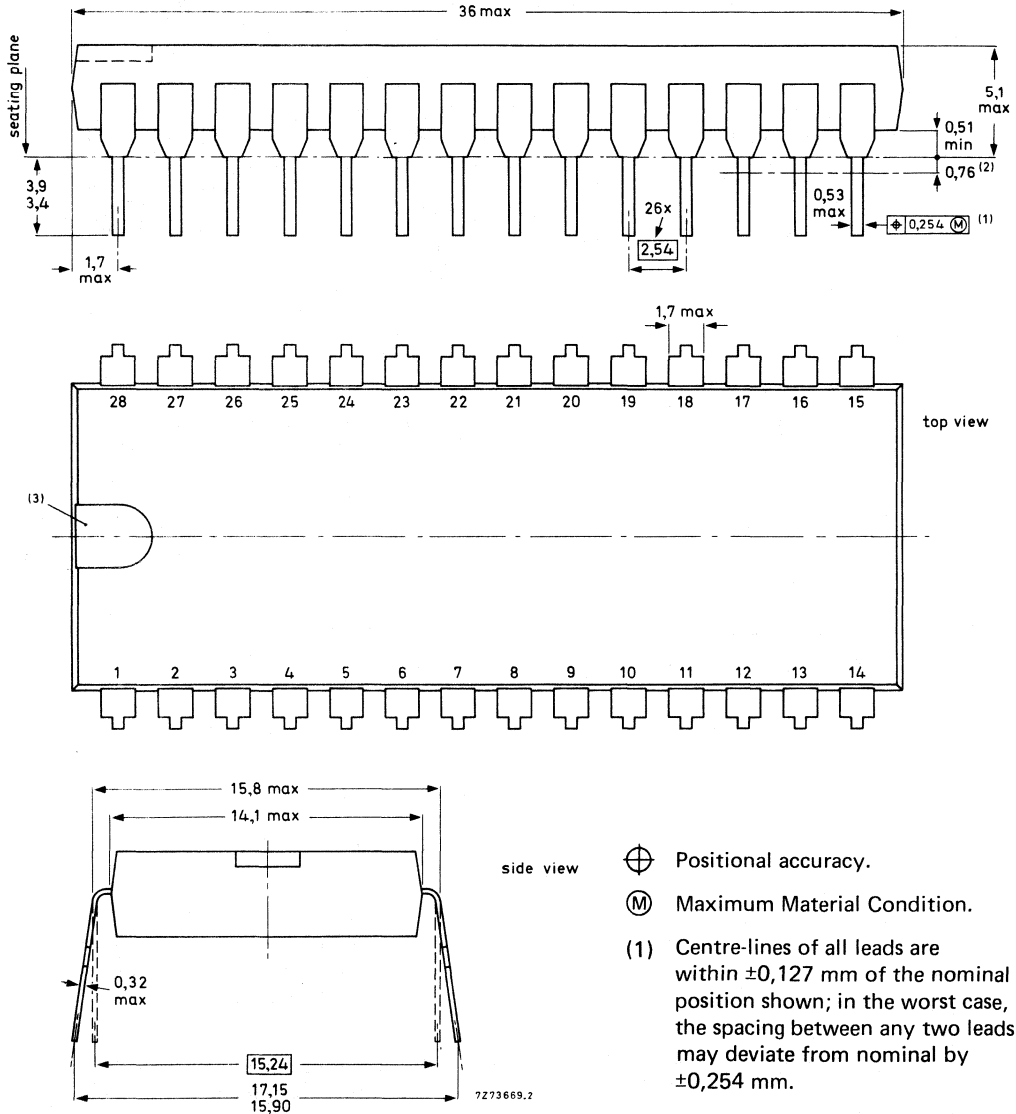
(1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING
See page 358

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



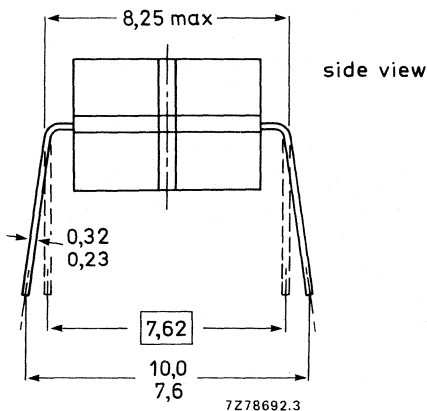
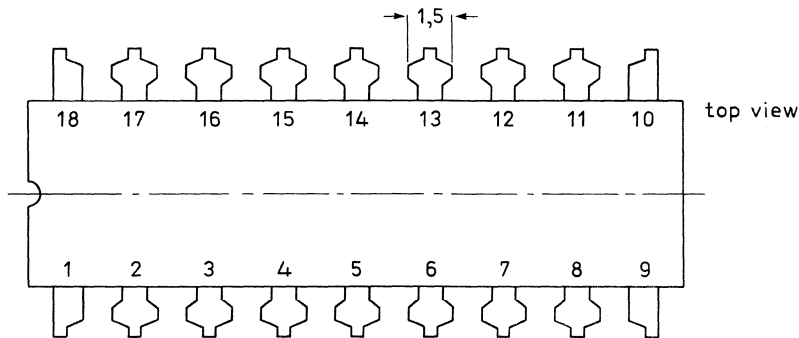
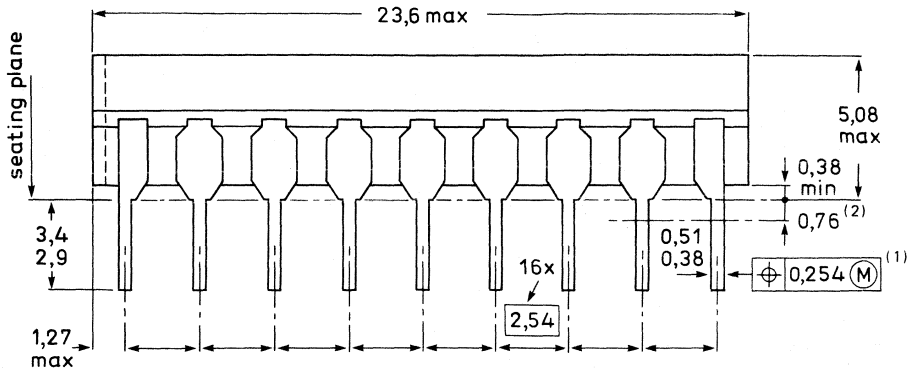
Dimensions in mm

SOLDERING
See page 358

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133B)



⊕ Positional accuracy.

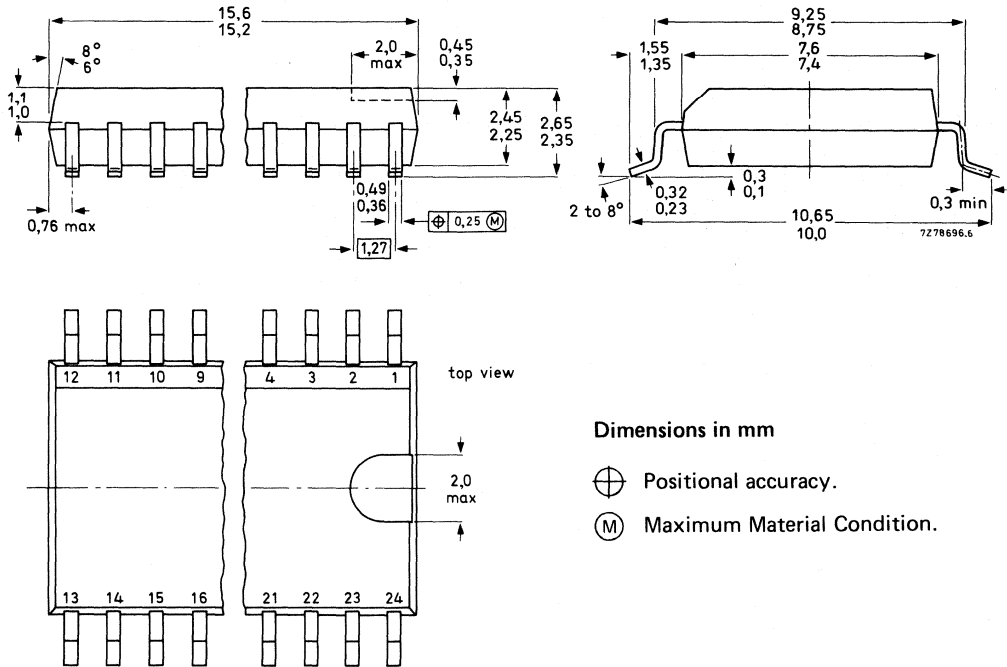
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO-24; SOT-137A)



SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

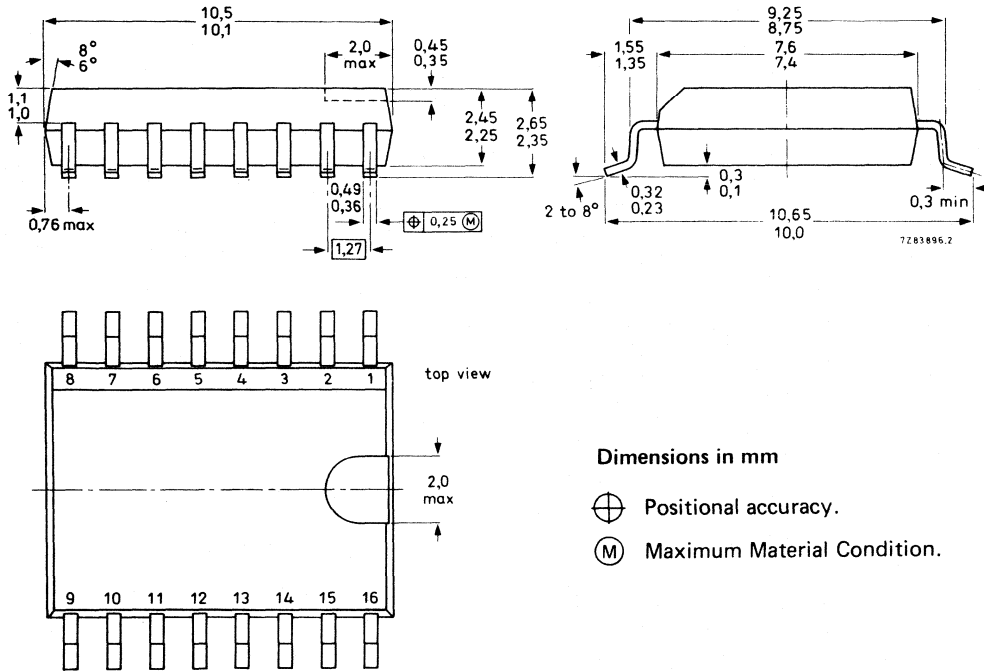
Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.

After soldering, the substrate must be cleaned of any remaining flux.

16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)



SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

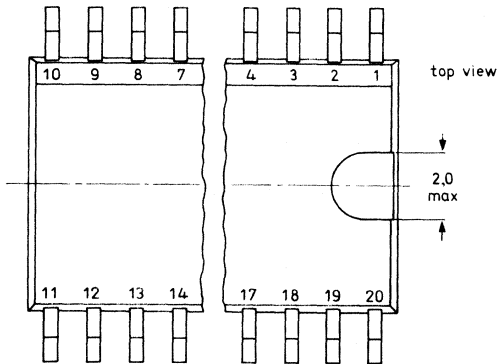
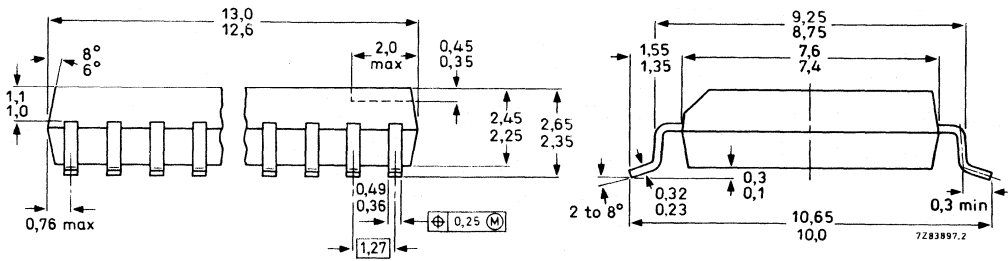
Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm . To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid. After soldering, the substrate must be cleaned of any remaining flux.

PACKAGE OUTLINES

20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)

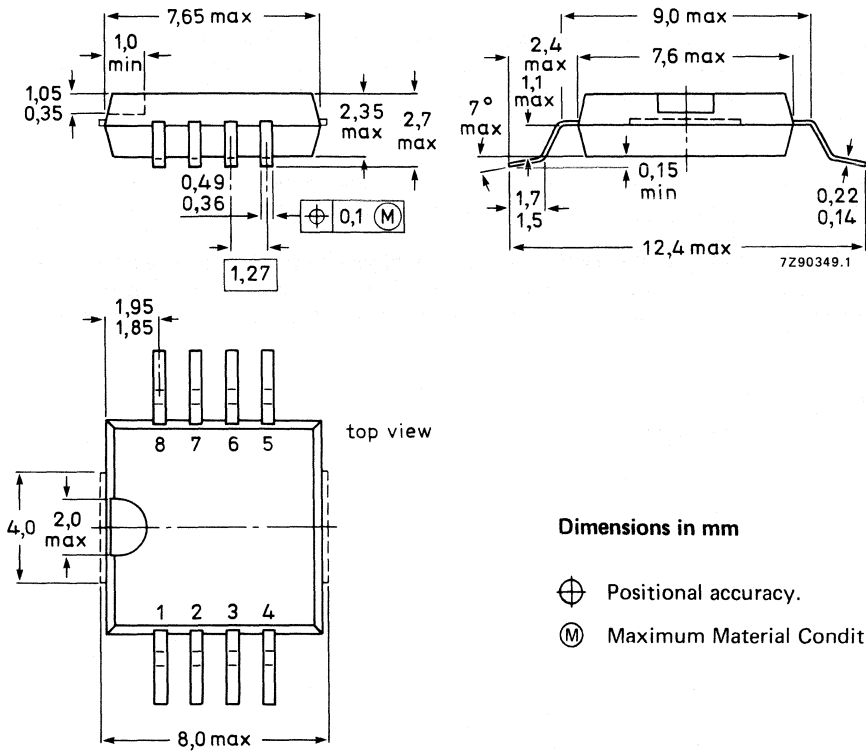


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

8-LEAD MINI-PACK; PLASTIC (SO-8L; SOT-176)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).

If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

Electronic components and materials for professional, industrial and consumer uses from the world-wide Philips Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Elcoma, Vedia 3892, 1430 BUENOS AIRES, Tel. 541-7141/7242/7343/7444/7545.
Australia: PHILIPS INDUSTRIES HOLDINGS LTD., Elcoma Division, 11 Waltham Street, ARTARMON, N.S.W. 2064, Tel. (02) 439 3322.
Austria: ÖSTERREICHISCHE PHILIPS BAUELEMENTE INDUSTRIE G.m.b.H., Triester Str. 64, A-1101 WIEN, Tel. 62 91 11-0.
Belgium: N.V. PHILIPS & MBLE ASSOCIATED, 9 rue du Pavillon, B-1030 BRUXELLES, Tel. (02) 2427400.
Brazil: IBRAPE, Caixa Postal 7383, Av. Brigadeiro Faria Lima, 1735 SAO PAULO, SP, Tel. (011) 211-2600.
Canada: PHILIPS ELECTRONICS LTD., Elcoma Division, 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. 39-4001.
Colombia: IND. PHILIPS DE COLOMBIA S.A., c/o IPRELENCO LTD., Cra. 21, No. 56-17, BOGOTA, D.E., Tel. 2497624.
Denmark: MINIWATT A/S, Strandlodsvej 2, P.O. Box 1919, DK 2300 COPENHAGEN S, Tel. (01) 54 11 33.
Finland: OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. 17271.
France: RTC-COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. 43 38 80 00.
Germany (Fed. Republic): VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS HELLENIQUE S.A., Elcoma Division, 54, Syngrou Av., ATHENS 11742, Tel. 9215311/319.
Hong Kong: PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-245121.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Elcoma Dept., Band Box Building, 254-D Dr. Annie Besant Rd., BOMBAY - 400 025, Tel. 4930311/4930590.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan, JAKARTA - Selatan, Tel. 512572.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 693355.
Italy: PHILIPS S.p.a., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6752.1.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03) 230-1521.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. 794-5011.
Malaysia: PHILIPS MALAYSIA SDN. BERHAD, No. 4 Persiaran Barat, Petaling Jaya, P.O.B. 2163, KUALA LUMPUR, Selangor, Tel. 77 44 11.
Mexico: ELECTRONICA, S.A de C.V., Carr. México-Toluca km. 62.5, TOLUCA, Edo. de México 50140, Tel. Toluca 91 (721) 613-00.
Netherlands: PHILIPS NEDERLAND, Marktgroep Elenco, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 793333.
New Zealand: PHILIPS NEW ZEALAND LTD., Elcoma Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. 605-914.
Norway: NORSK A/S PHILIPS, Electronica Dept., Sandstuveien 70, OSLO 6, Tel. 68 02 00.
Peru: CADESA, Av. Alfonso Ugarte 1268, LIMA 5, Tel. 326070.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. 86-89-51 to 59.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. 68 31 21.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 3502000.
South Africa: EDAC (PTY.) LTD., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001, Tel. 614-2362/9.
Spain: MINIWATT S.A., Balmes 22, BARCELONA 7, Tel. 301 63 12.
Sweden: PHILIPS KOMPONENTER A.B., Lidingövägen 50, S-11584 STOCKHOLM 27, Tel. 08/7821000.
Switzerland: PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. 01-488 22 11.
Taiwan: PHILIPS TAIWAN LTD., 150 Tun Hua North Road, P.O. Box 22978, TAIPEI, Taiwan, Tel. 7120500.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., Elcoma Department, İnönü Cad, No. 78-80, P.K.504, 80074 ISTANBUL, Tel. 4359 10.
United Kingdom: MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. 01-580 6633.
United States: (Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive Devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201) 539-2000.
(Passive Devices & Electromechanical Devices) CENTRALAB INC., 5855 N. Glen Park Rd., MILWAUKEE, WI 53201, Tel. (414)228-7380.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 991-2000.
Uruguay: LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. 91 43 21.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., c/o MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, App. Post. 78117, CARACAS, Tel. (02) 2393931.

For all other countries apply to: Philips Electronic Components and Materials Division, International Business Relations, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Telex 35000 phtnl